


INTERNAL ONLY

BPAGE DRAWING

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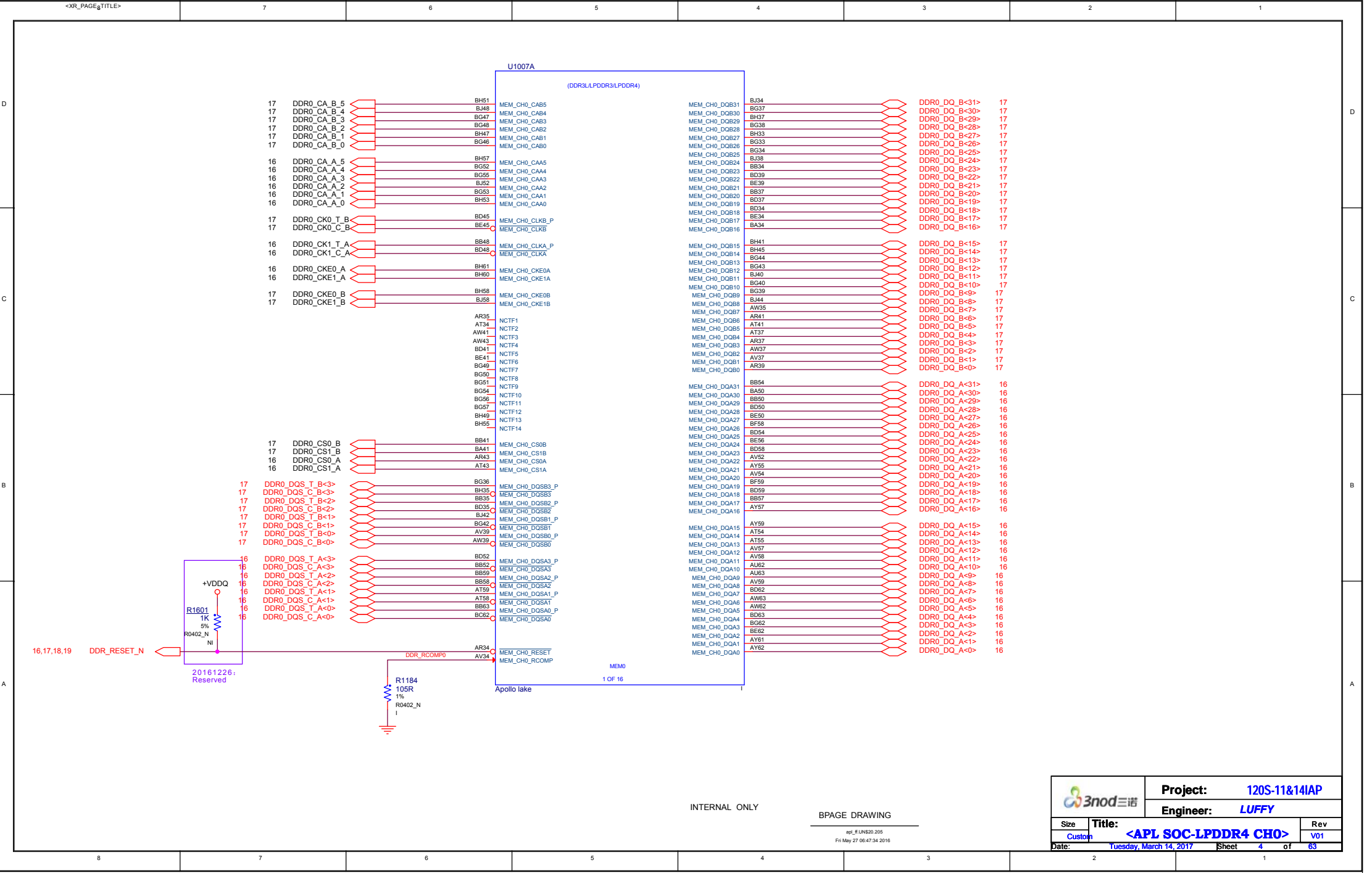
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		<b>Project:</b> 120S-11&14IAP		
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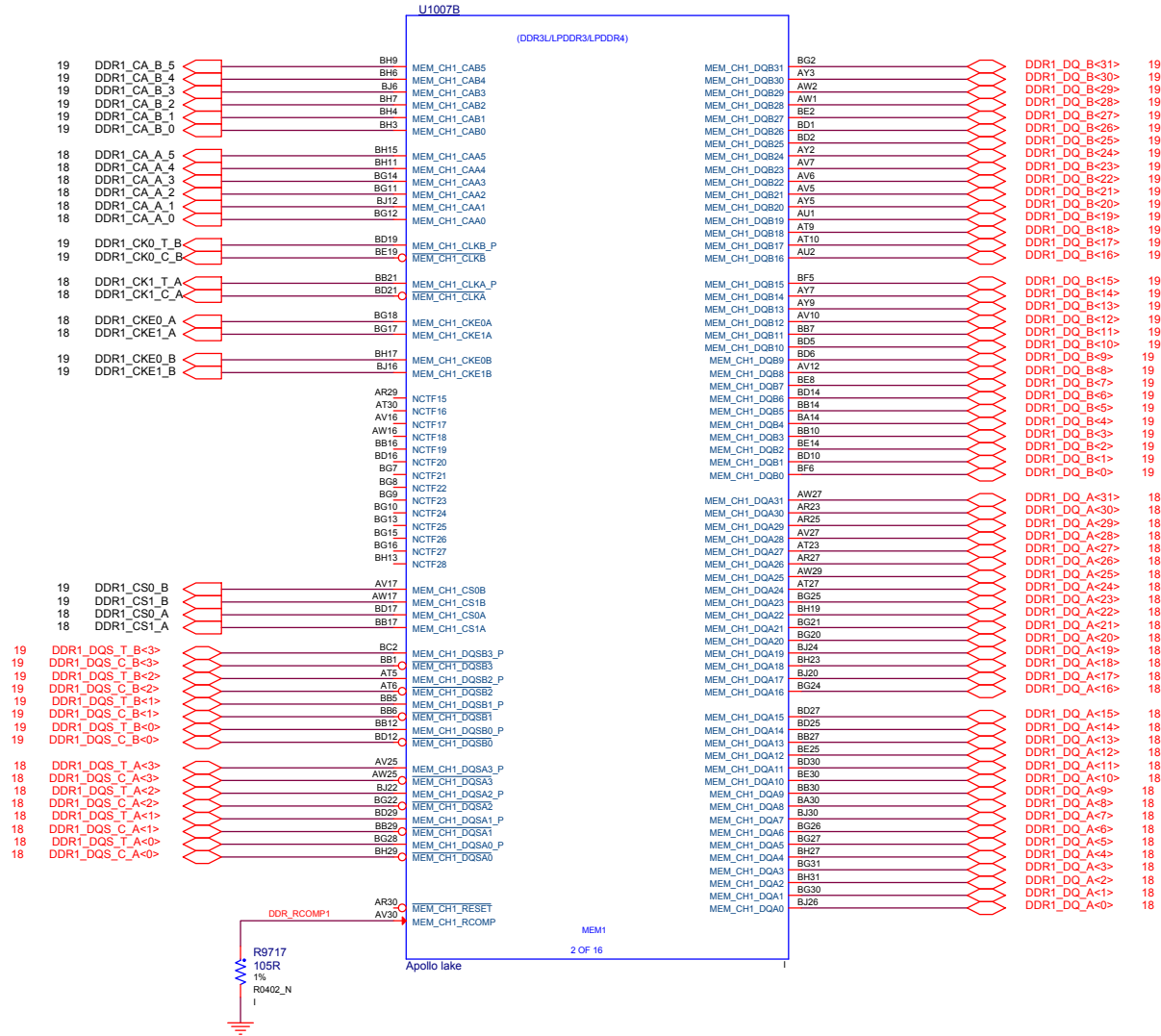
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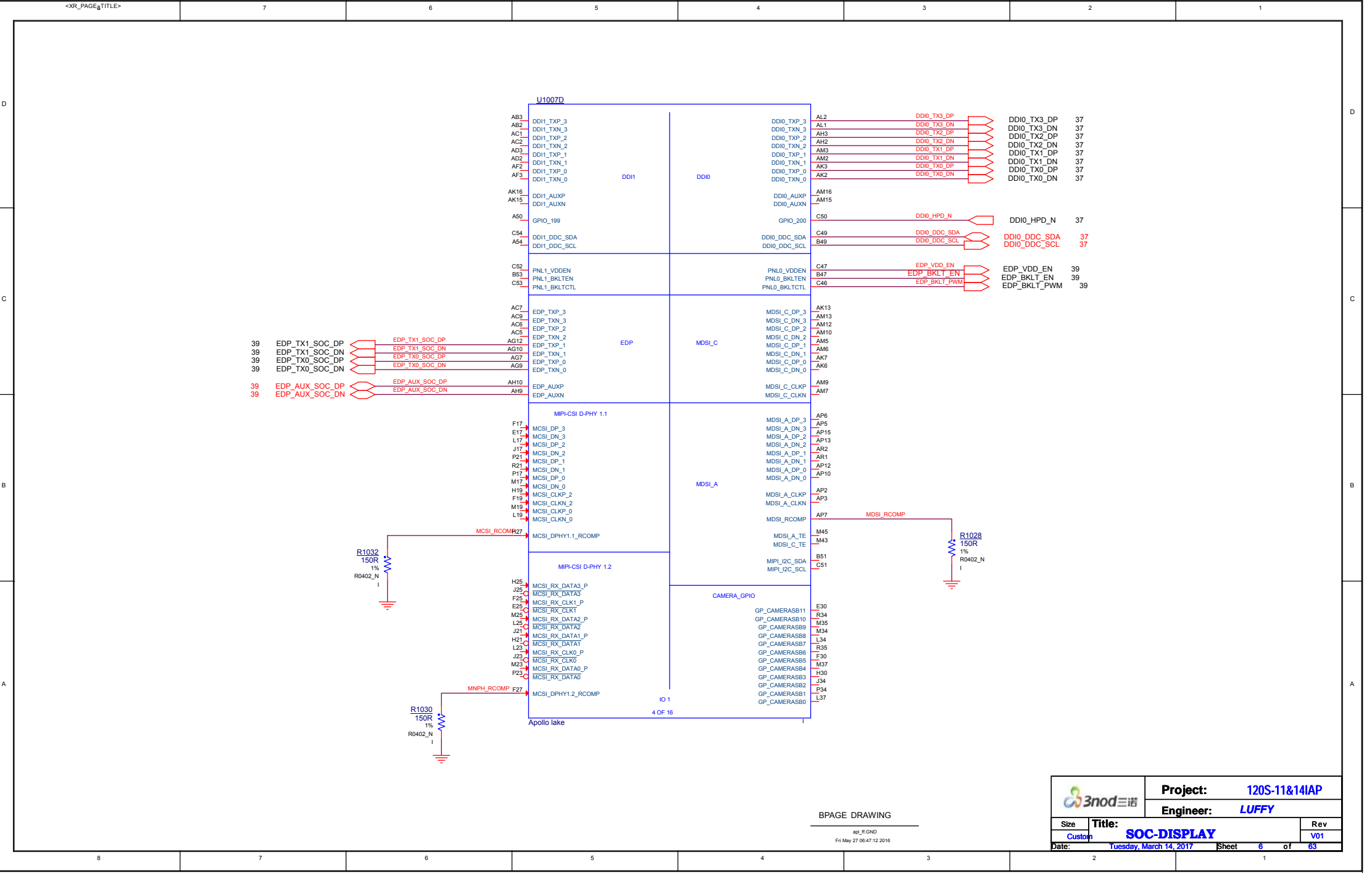
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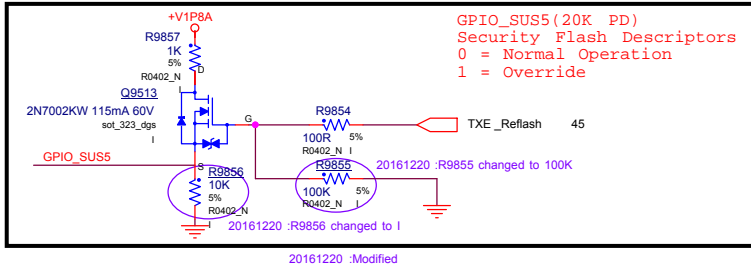
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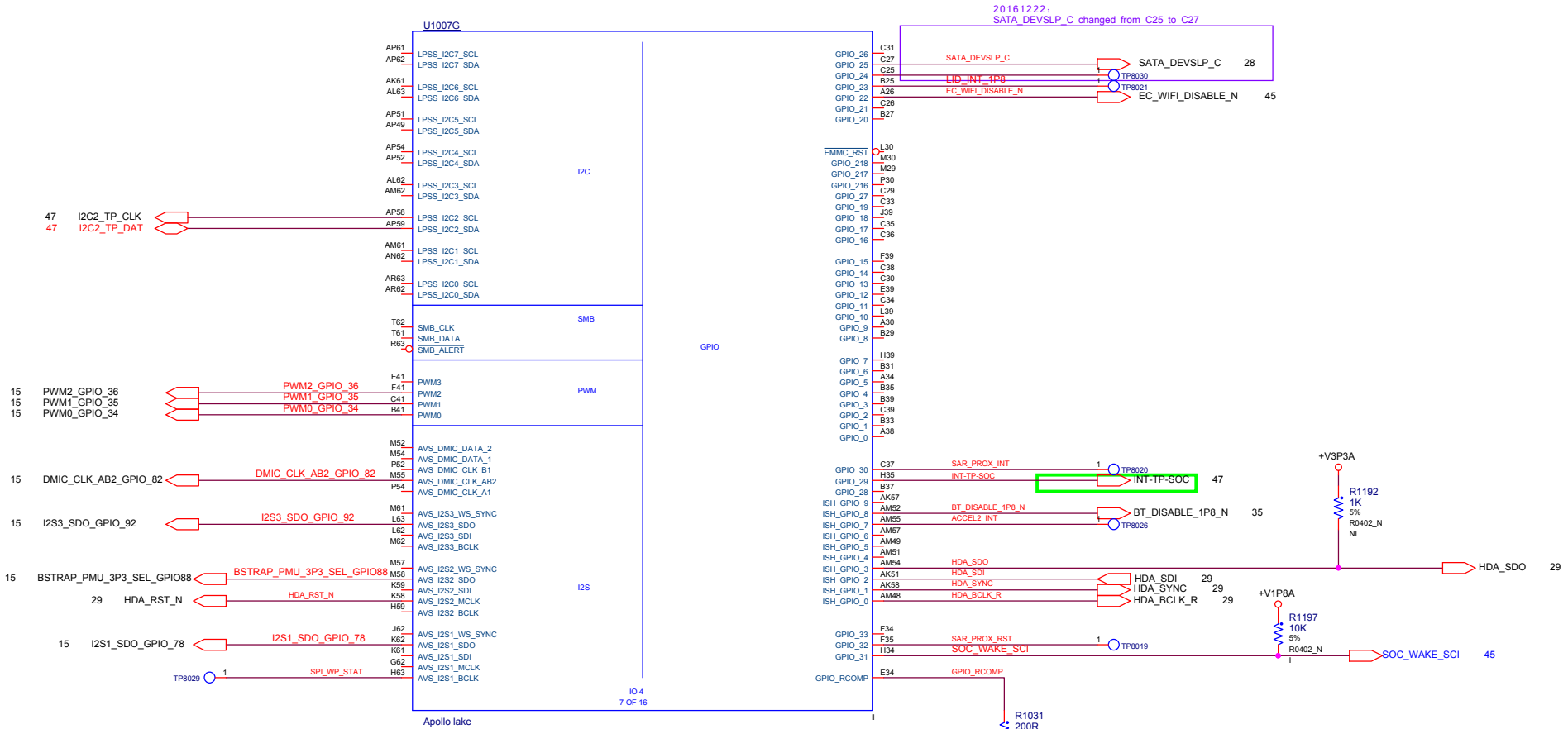
R1199 - EMMC BOOT STRAP



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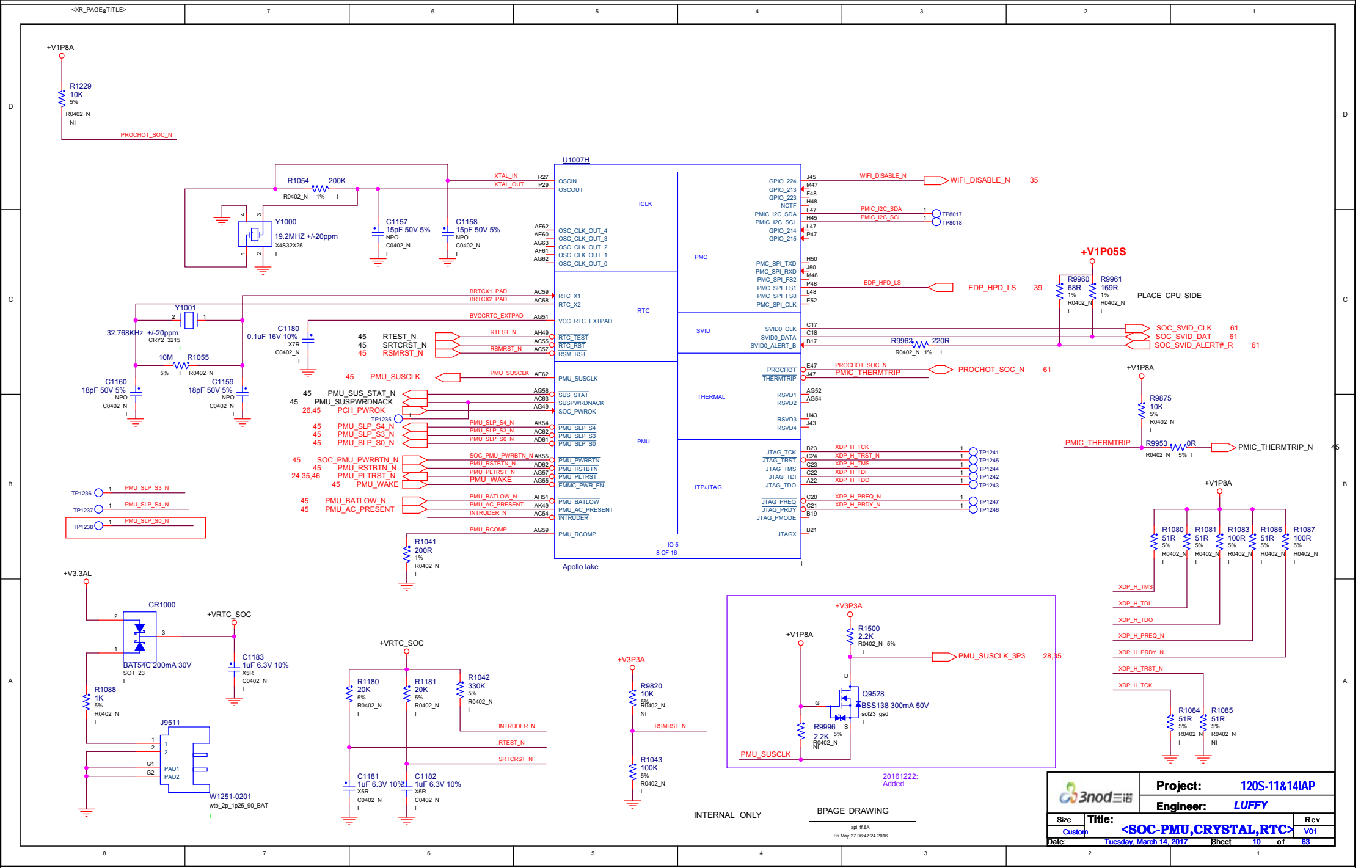
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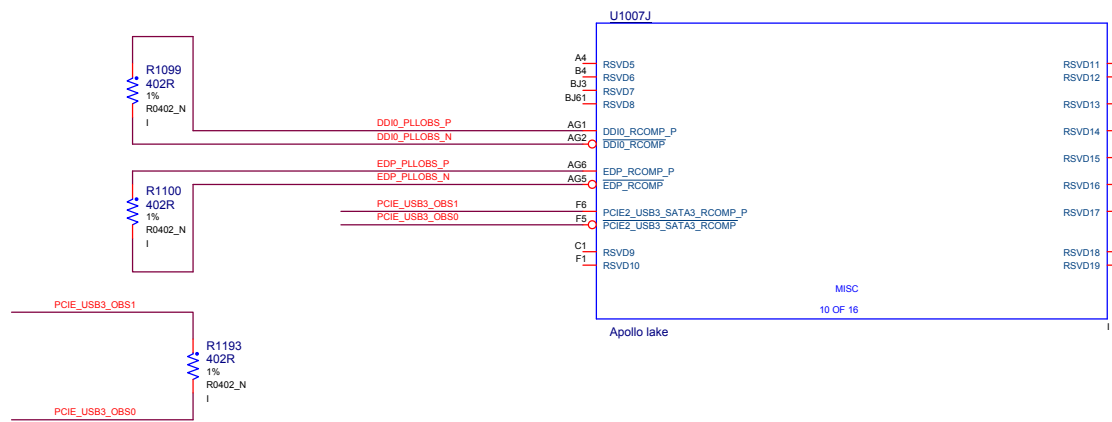
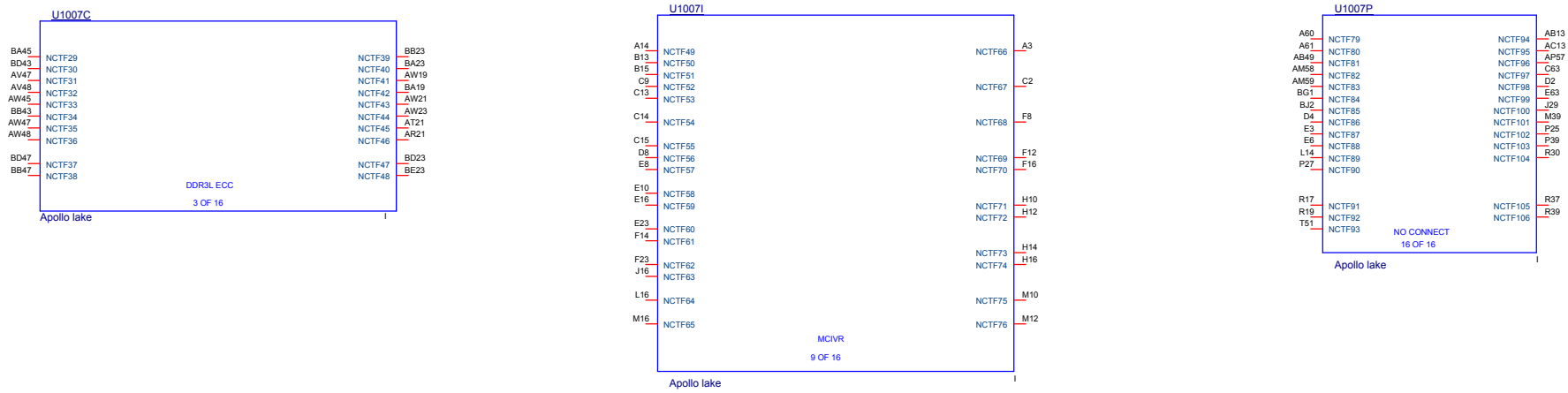
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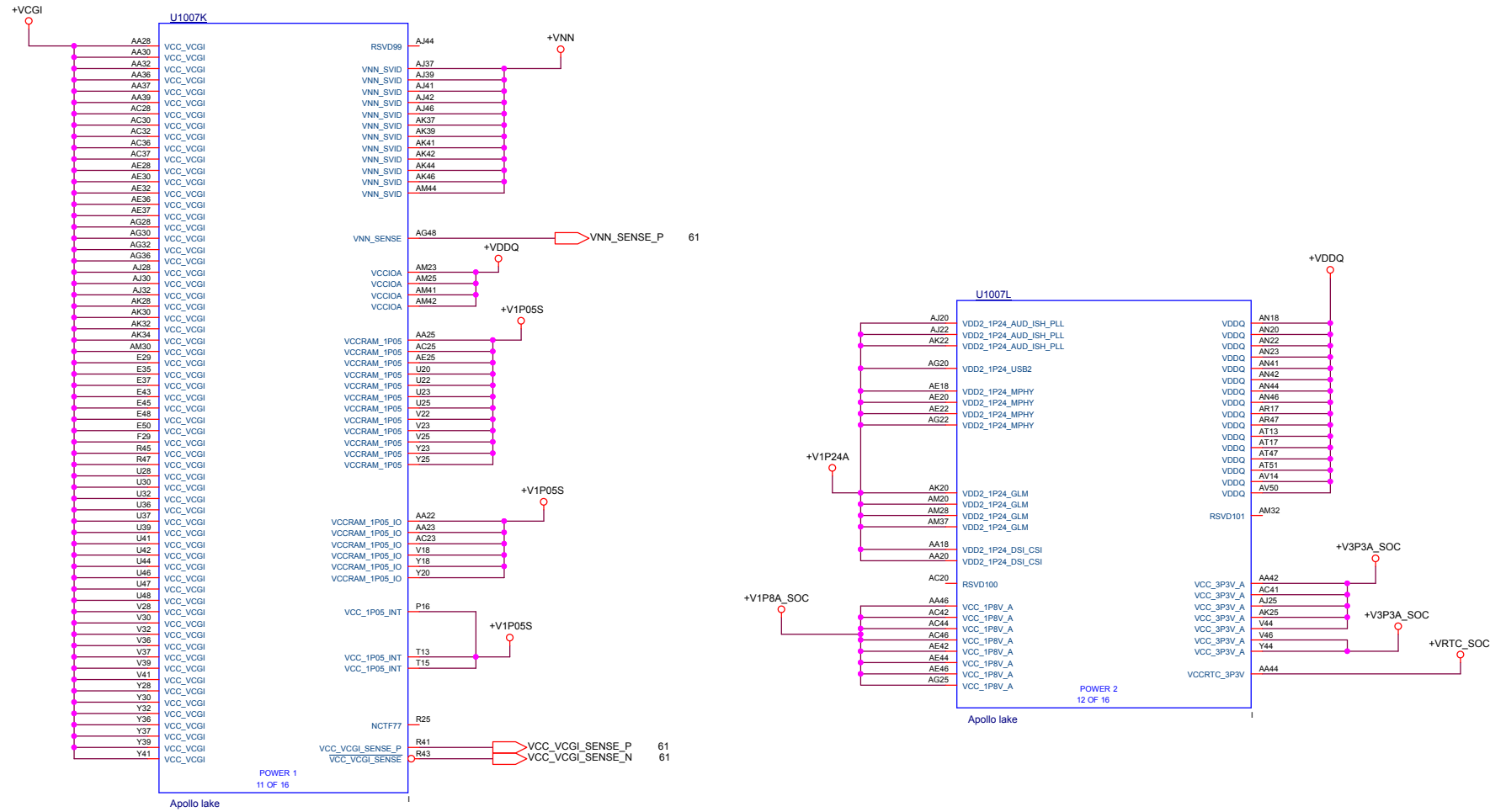
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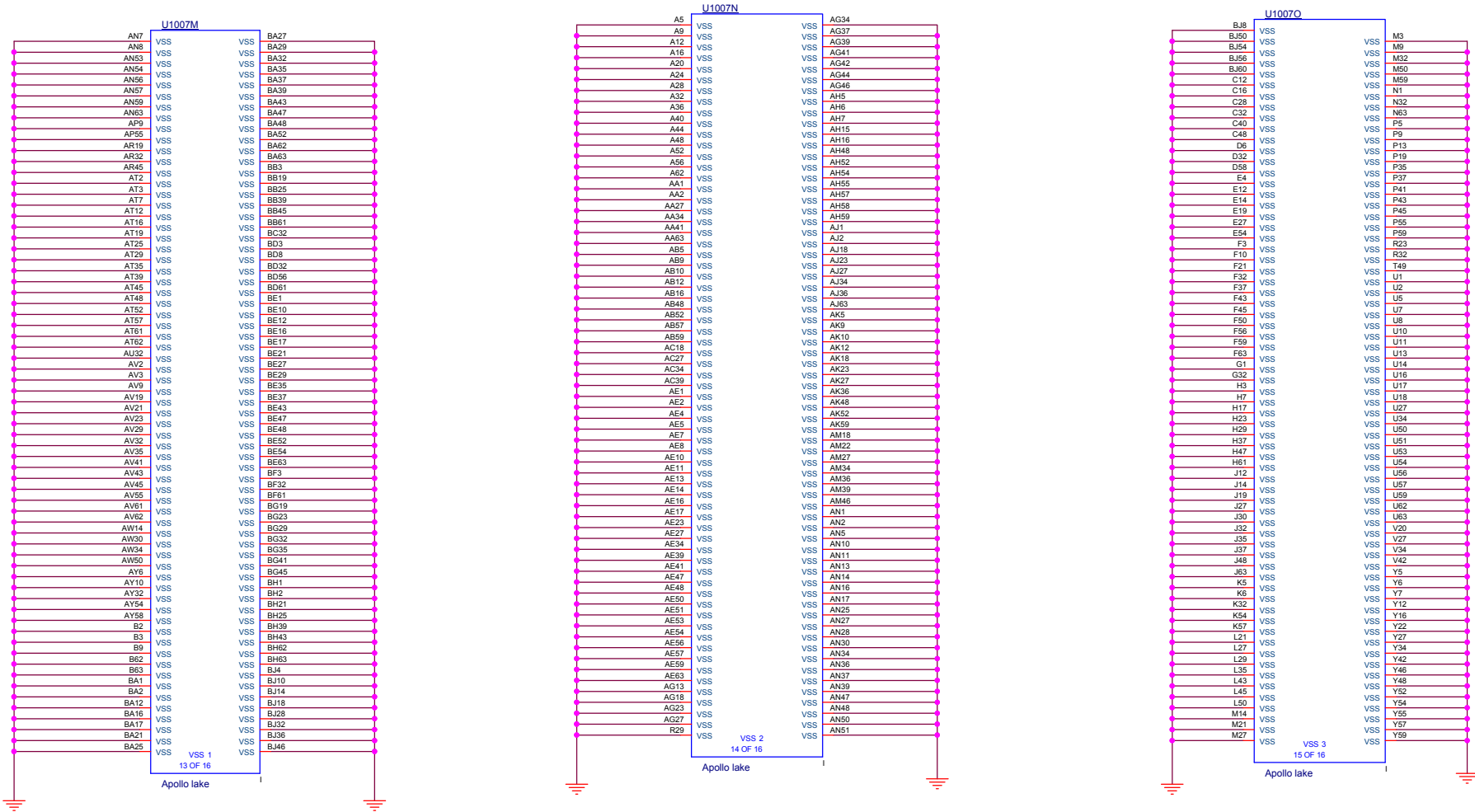


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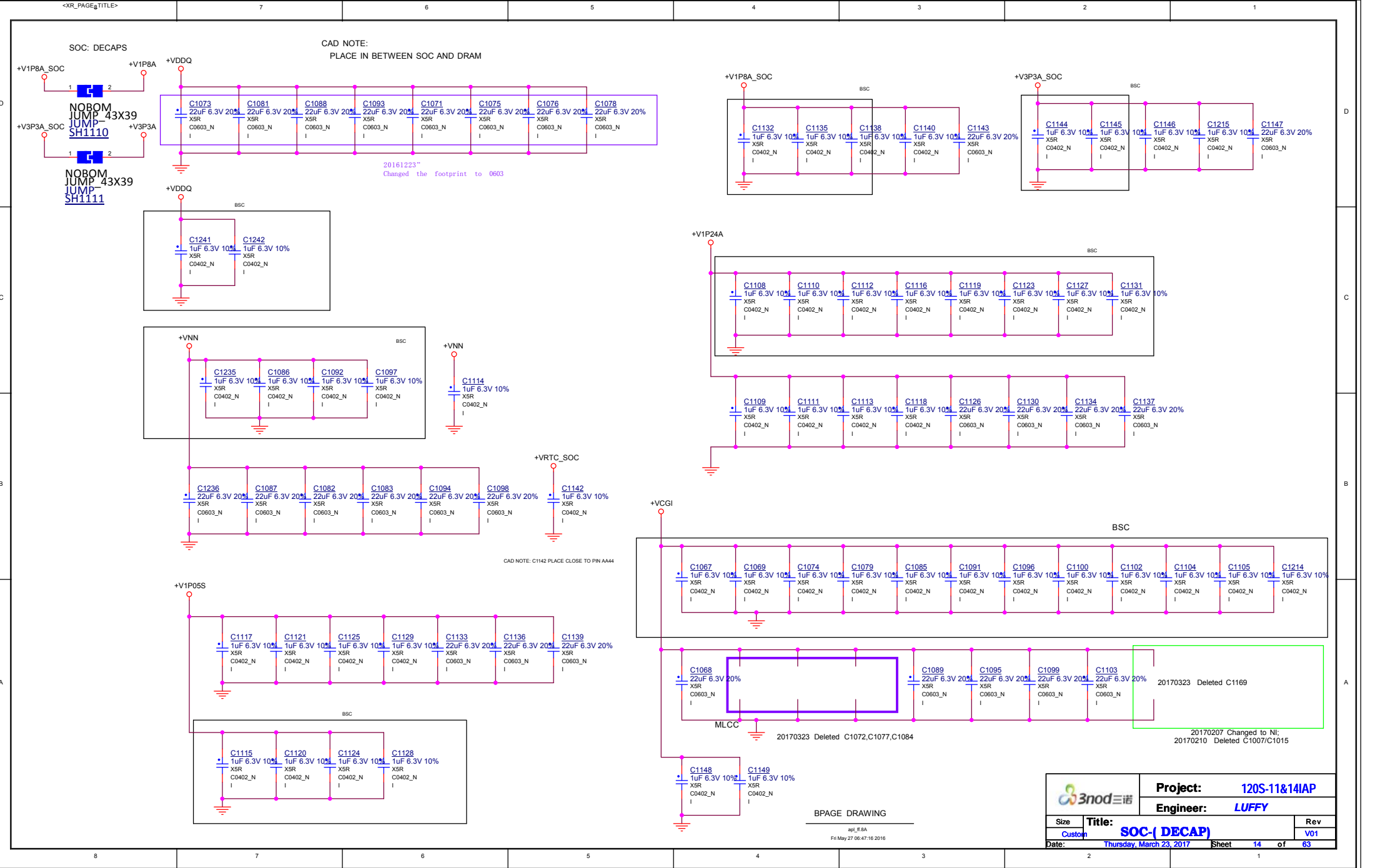
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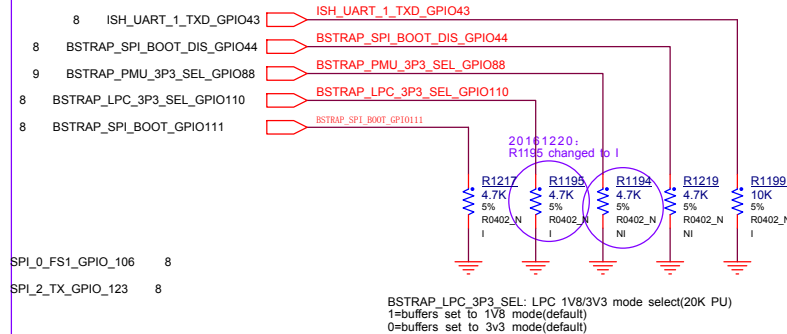
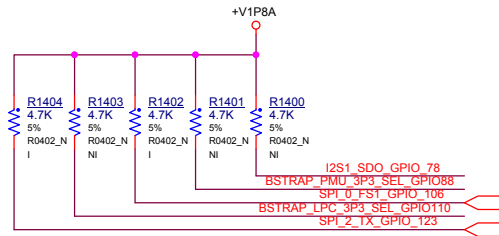
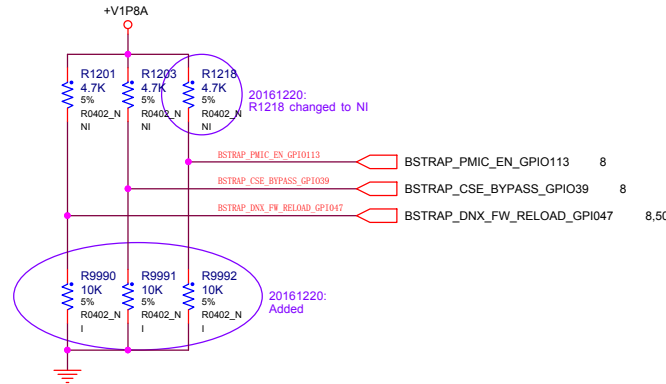
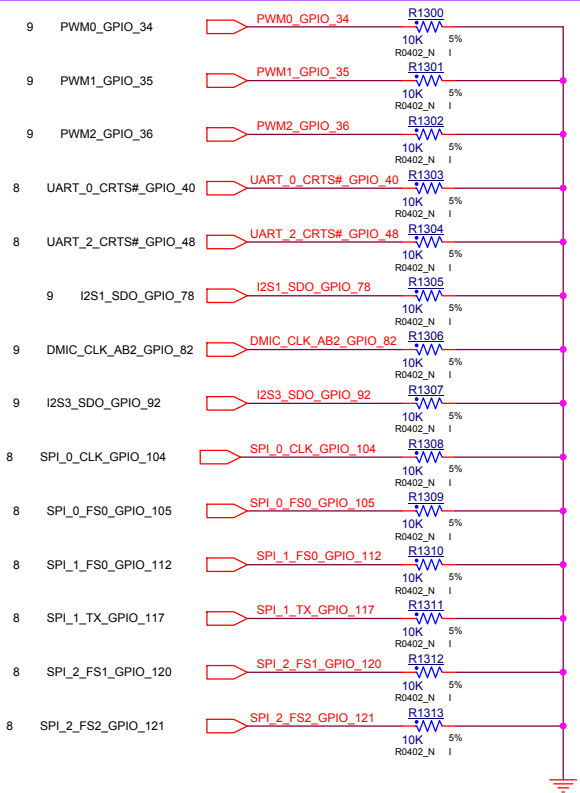
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BXT-P GPIO	SOC Ball Name	BSTRAP	Default Internal PU/PD
GPIO34	PWM0	Delayed_vref_switch 0= not delayed(Default) 1=delayed	PD
GPIO35	PWM1	Spare1 0= do not stall boot FSM(Default) 1=stall boot FSM	PD
GPIO36	PWM2	Spare2 0 =VDD2 IS 1.24V(Default) 1=VDD2 IS 1.35V	PD
GPIO39	LPASS_UART0_TXD	Enable CSE ROM bypass 0 = disable bypass (default) 1 = enable bypass	PD
GPIO40	RTC Clock Timer Bypass	RTC Clock Timer Bypass 0 =disable bypass (Default) 1 =enable bypass	PD
GPIO43	LPASS_UART1_TXD	Select eMMC boot source 0 =do not allow (Default) 1=allow	PU
GPIO44	LPASS_UART1_RTS_B	Select SPI boot source 0 =Disable 1=Enable(Default)	PU
GPIO47	LPASS_UART2_TXD	Force DNX FW Load 0 =Disable(Default) 1=Enable	PD
GPIO48	LPASS_UART2_RTS_B	LPC Boot strap 0 =Do not boot from LPC(Default) 1=Enable	PD
GPIO78	AVS_I2S1_SDO	SMBus 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO82	AVS_M_CLK_AB2	WC_PRESENT 0=non-Whiskey Cove(Default) 1=Whiskey Cove is connected	PD
GPIO88	AVS_I2S2_SDO	PMU (Power Management Unit) 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO92	AVS_I2S3_SDO	SMBus No Re-Boot 0=Disable(Default) 1=Enable	PD
GPIO104	GP_SSP_0_CLK	(HVM Tester)XTAL startup 0=Disable(Default) 1=Enable	PD
GPIO105	GP_SSP_0_FS0	(HVM Tester)XTAL startup 0=Disable(Default) 1=Enable	PU
GPIO106	GP_SSP_0_FS1	Halts early boot for debug 0=Enable 1=Disable	PU
GPIO110	GP_SSP_0_TXD	LPC 1.8V/3.3V mode select 0=buffers set to 3.3V mode 1=buffers set to 1.8V mode (default)	PU
GPIO111	GP_SSP_1_CLK	SPI Boot BIOS strap 0=boot from SPI(Debug) 1=Do not boot from SPI (default)	PU
GPIO112	GP_SSP_1_FS0	Enable metal password auth 0=Disable 1=Enable	PD
GPIO113	GP_SSP_1_FS1	SVID diable 0=Enable SVID(Default) 1=Disbale SVID	PU
GPIO117	GP_SSP_1_TXD	Stall B0ot FSM for debut 0=Do not stall boot FSM(Default) 1=stall boot FSM	PD
GPIO118	GP_SSP_2_CLK	Flash Descriptpr Override Pin-Strap status 0=Disable(Default) 1=Enable	PD
GPIO120	GP_SSP_2_FS1	Top swap pverride 0=Disable(Default) 1=Enable	PD
GPIO121	GP_SSP_2_FS2	Pilled LOW when RSM_RST_N deasserts	PD
GPIO123	GP_SSP_2_TXD	Pulled HIGH when RSM_RST_N de-asserts	PU

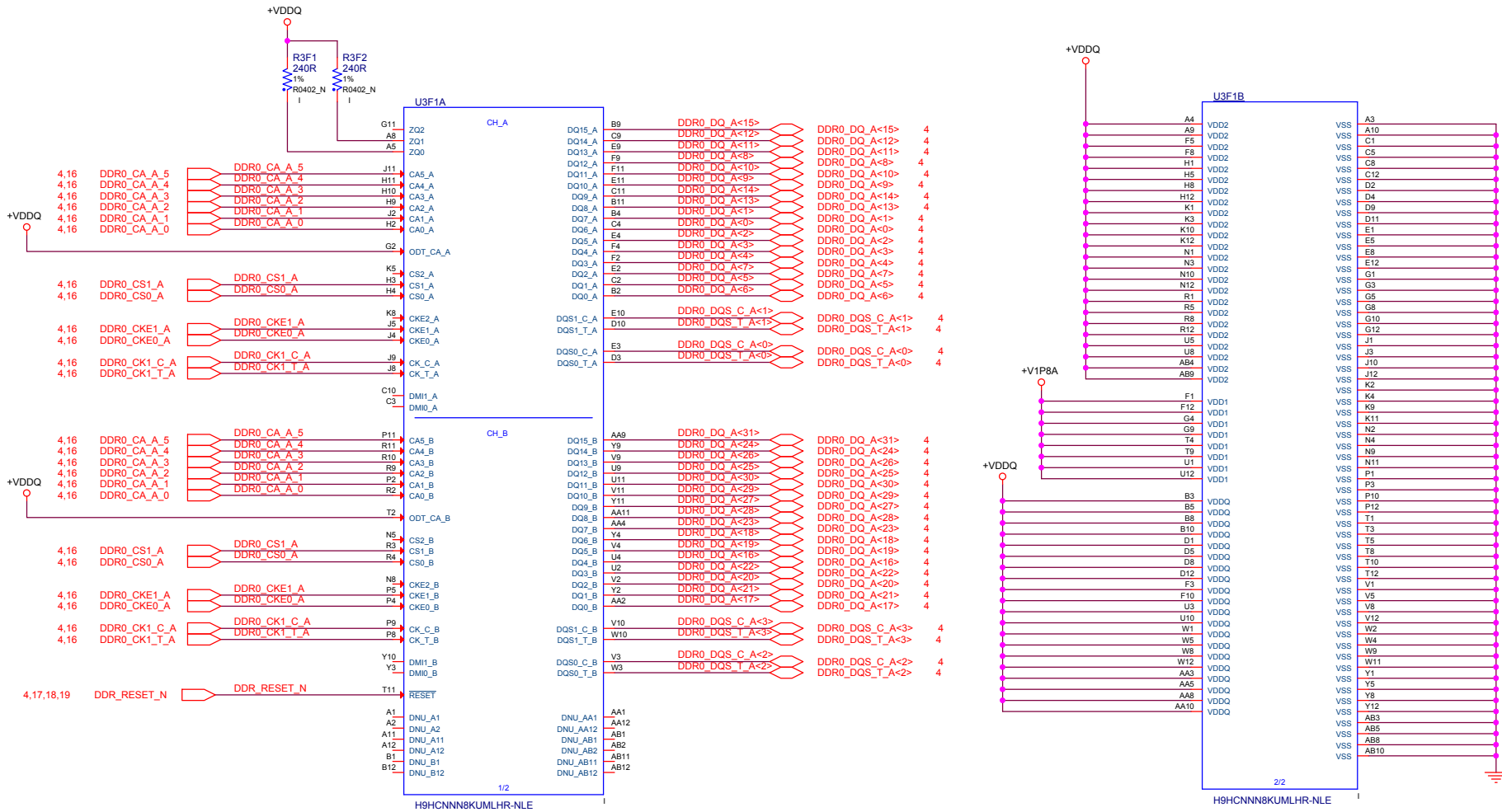
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CHANNEL 0 - MEMORY1/2

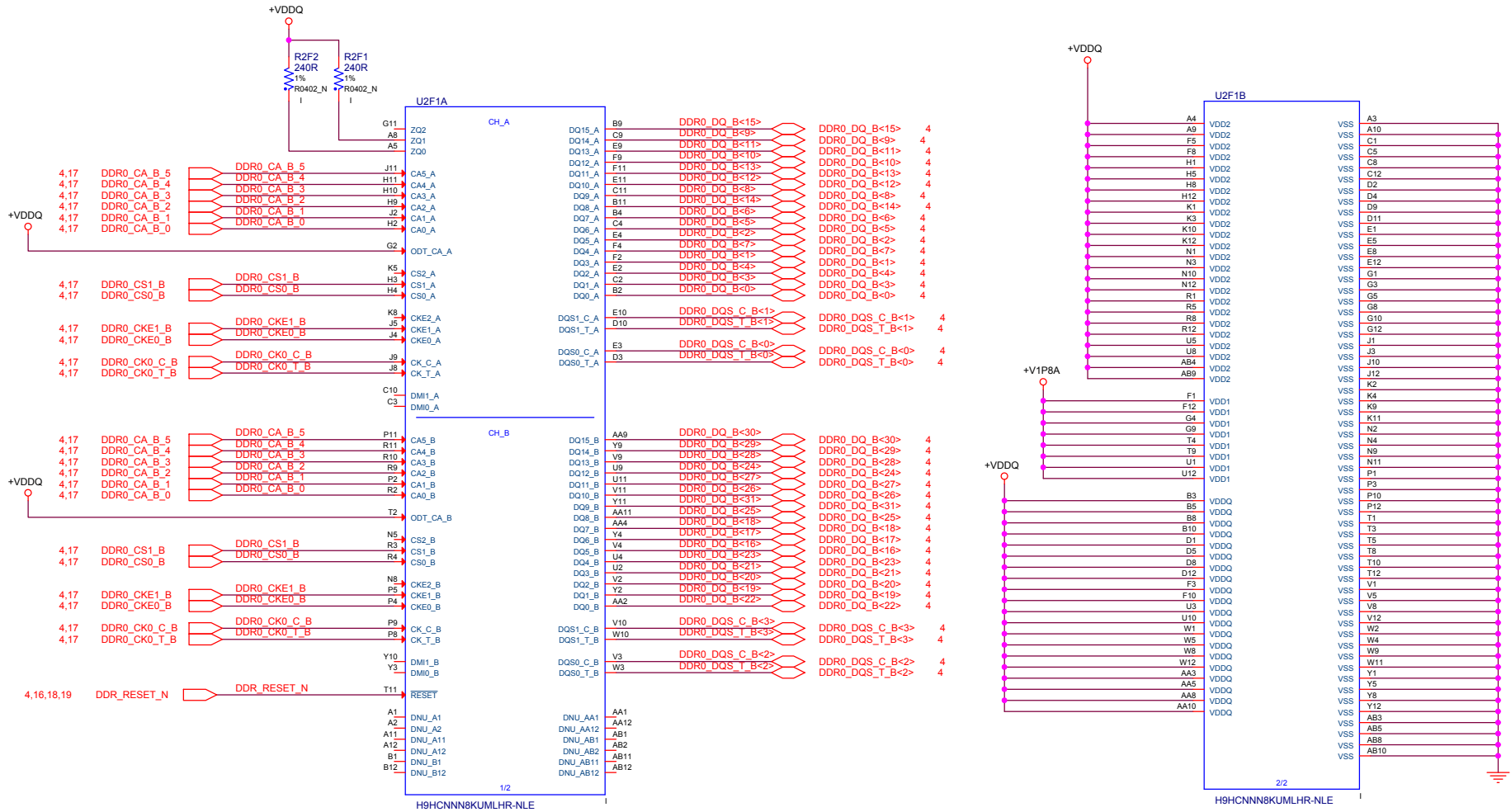


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CHANNEL 0 - MEMORY2/2

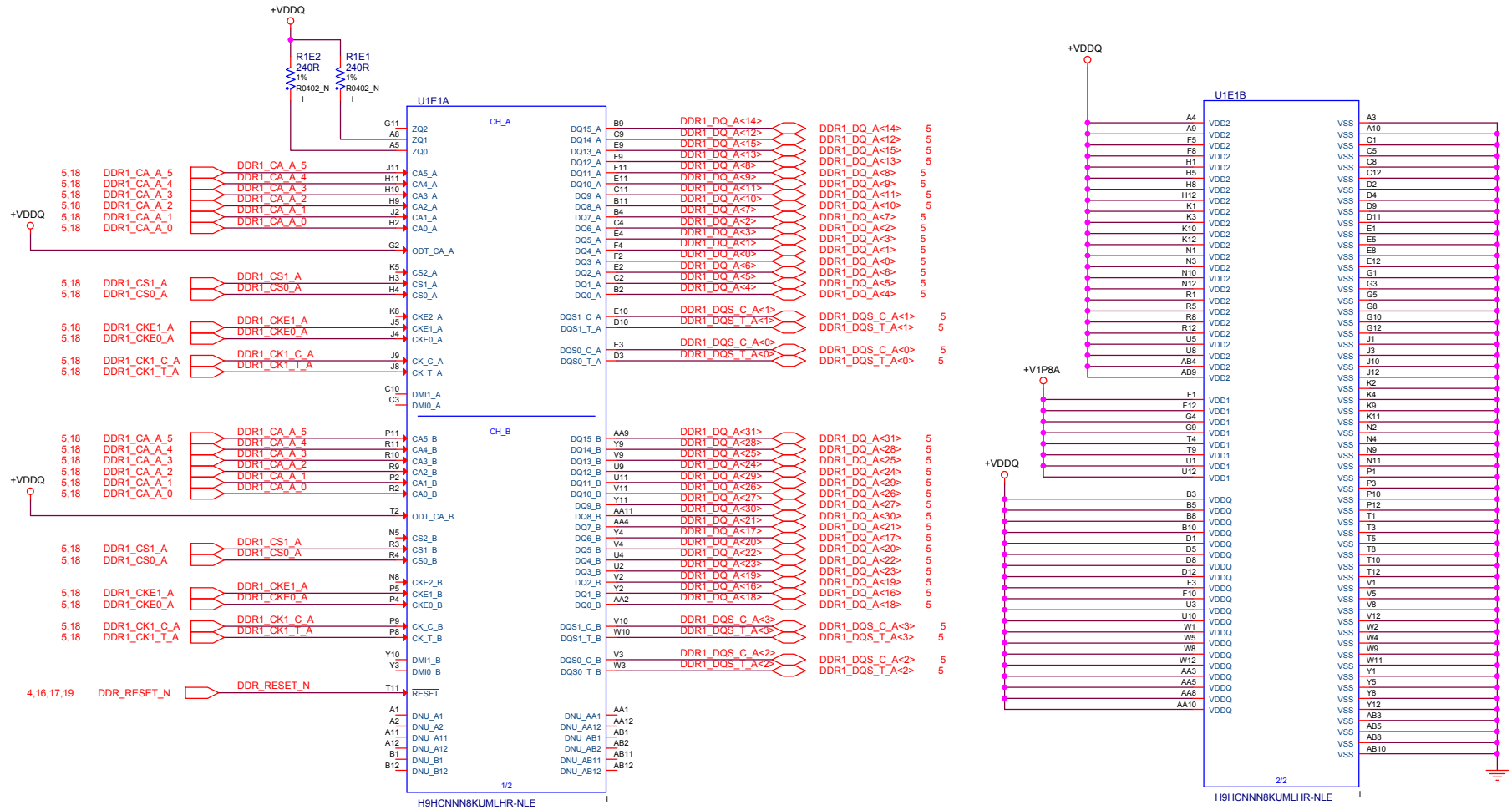


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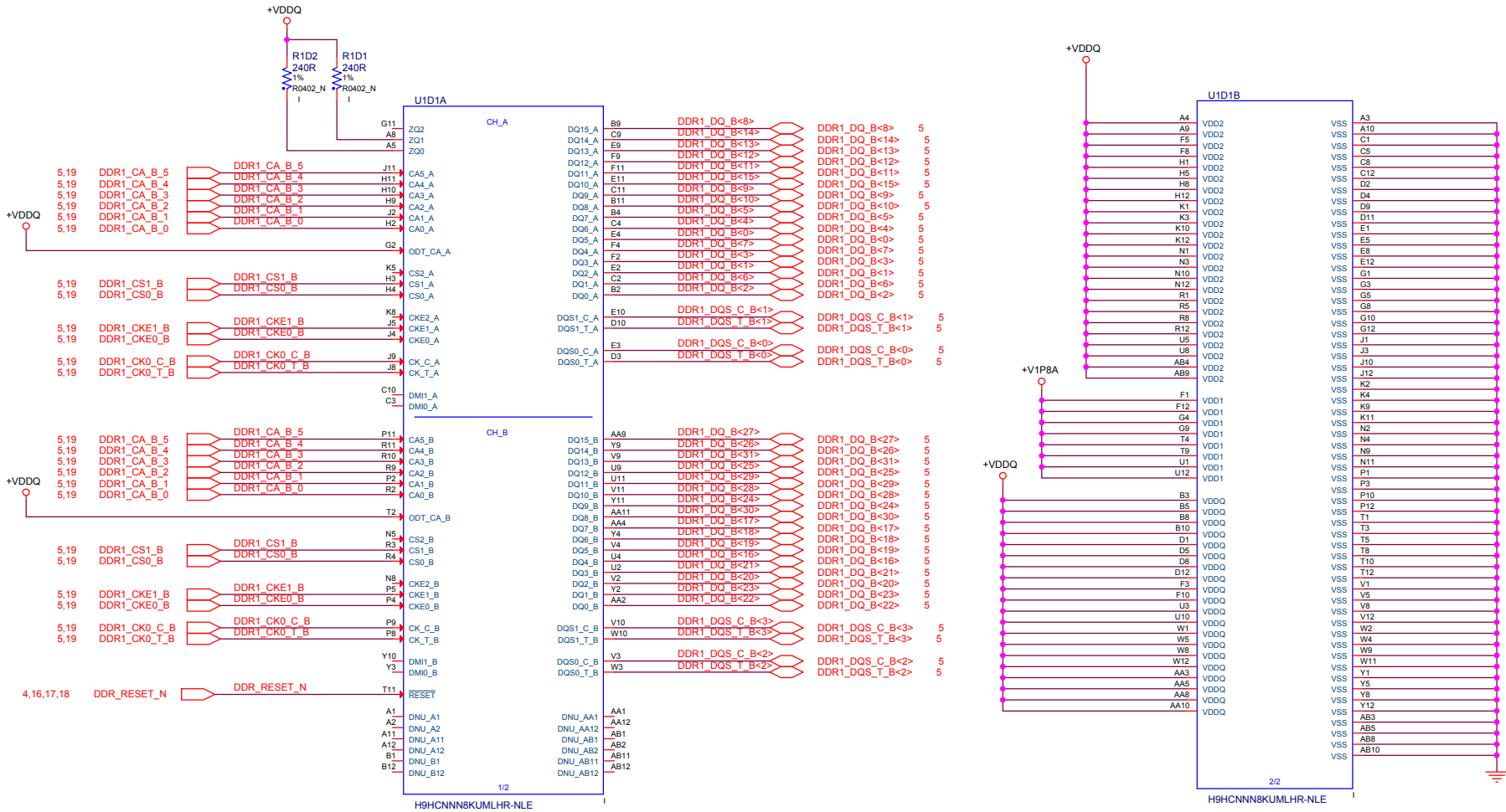
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# CHANNEL 1 - MEMORY2/2



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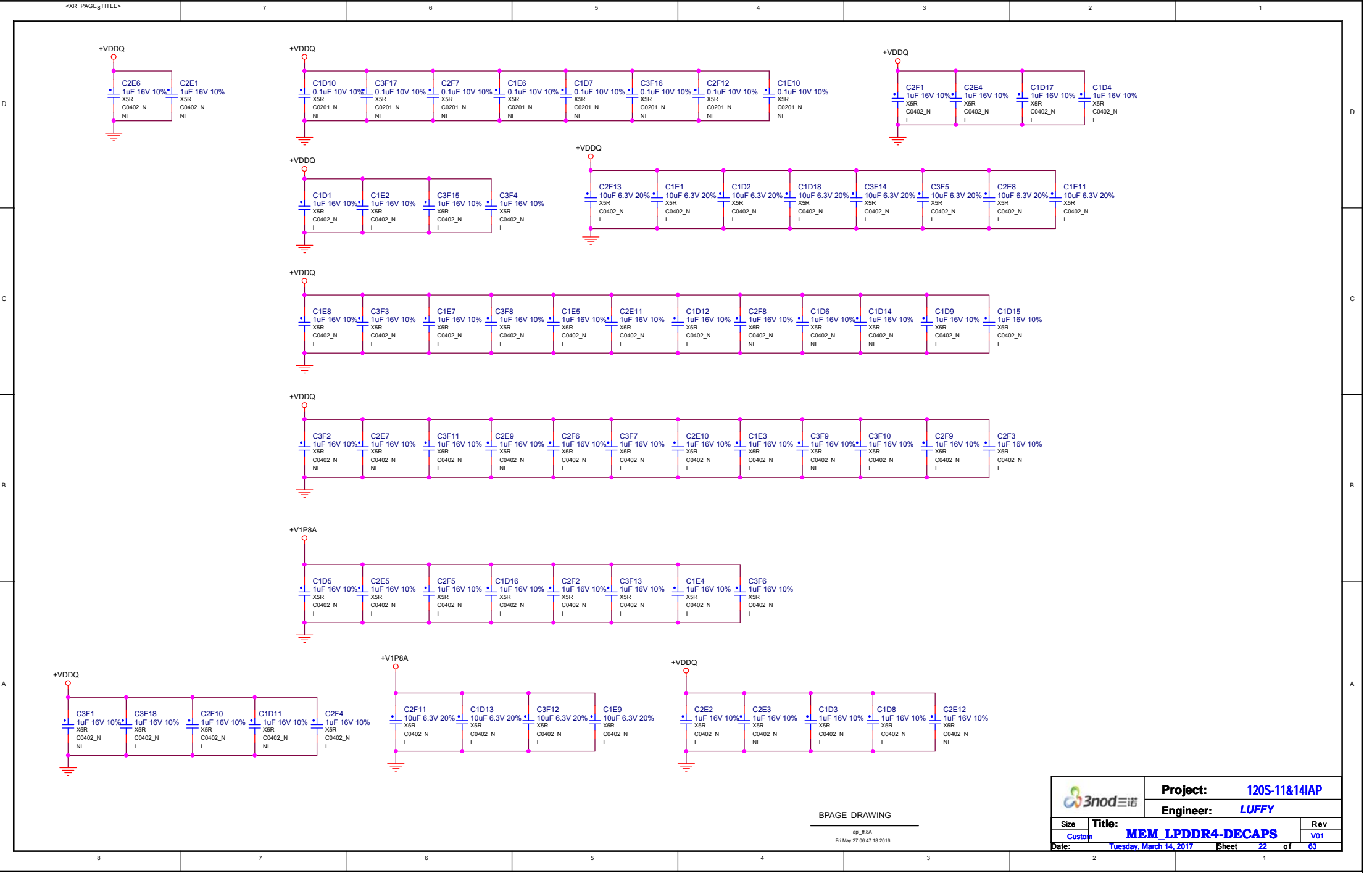
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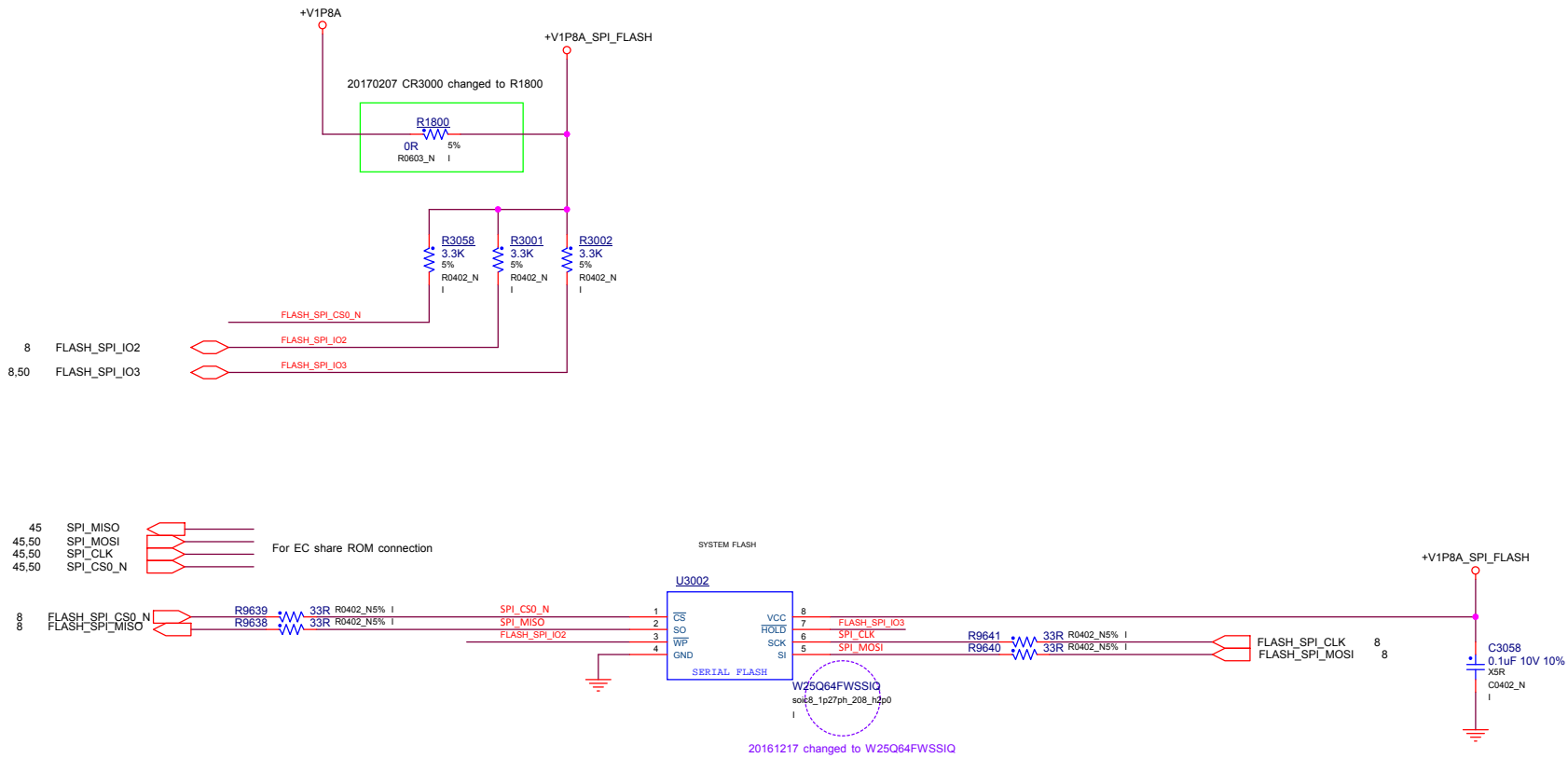
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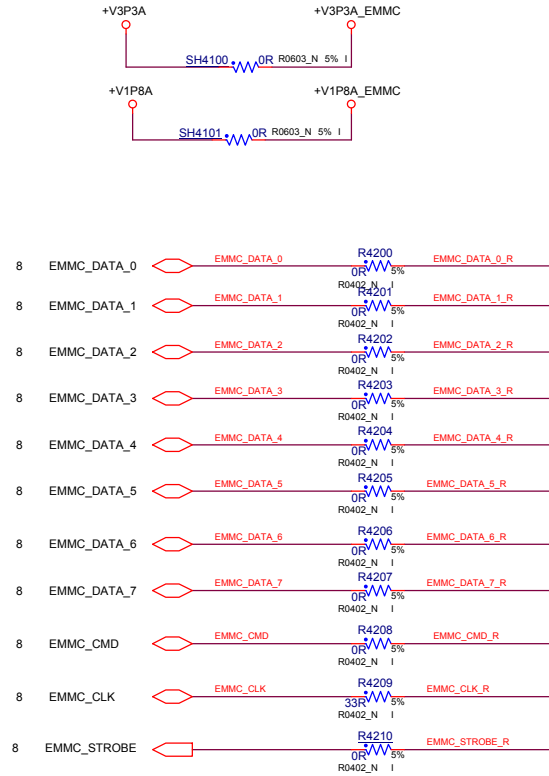
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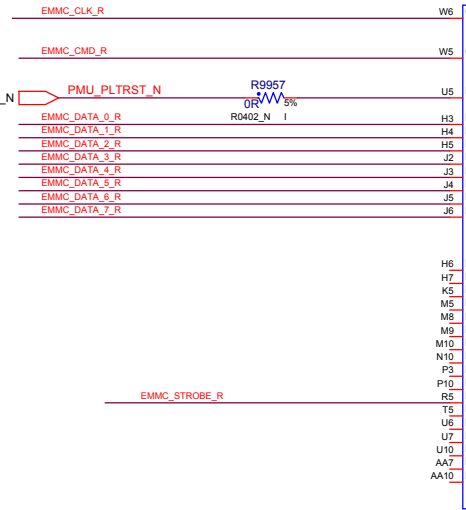
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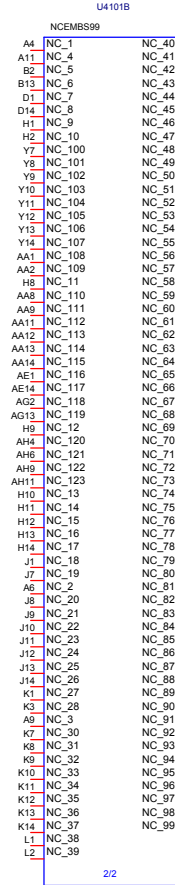
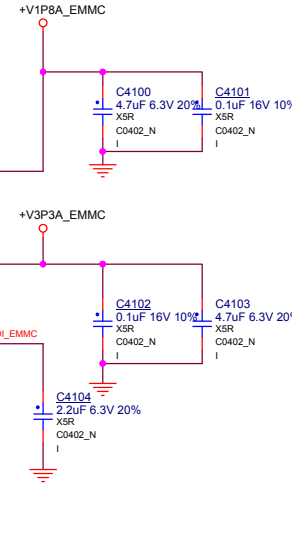
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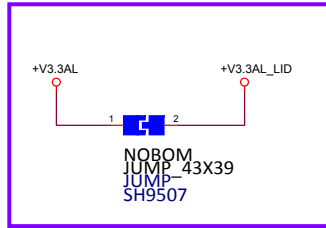
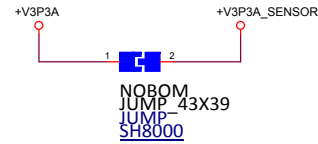


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### SENSORS



20170316 Added

### CPU THERMAL SENSOR

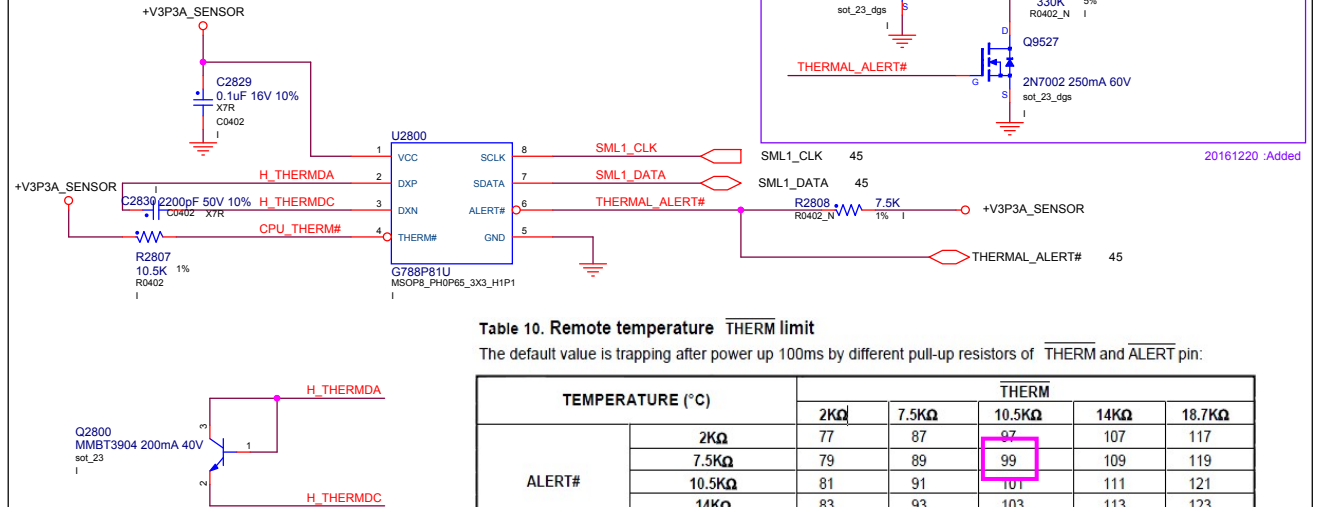
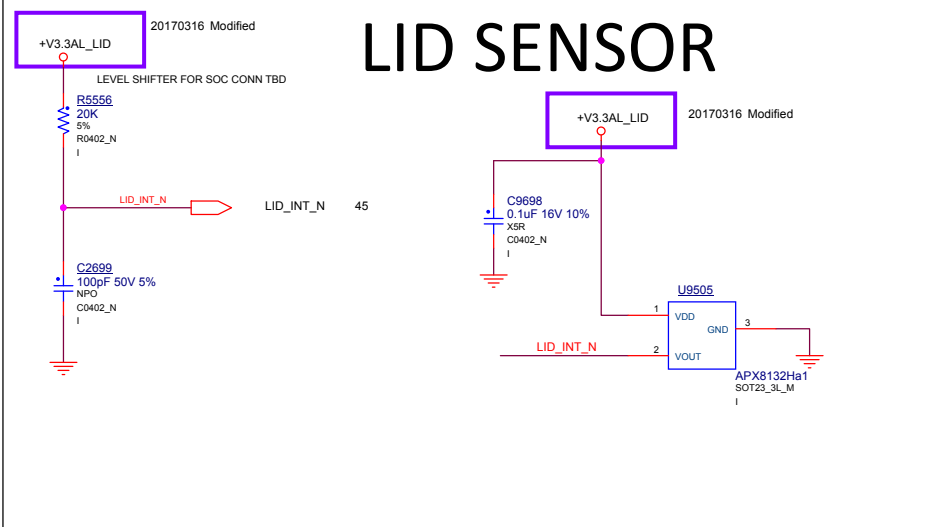


Table 10. Remote temperature THERM limit

The default value is trapping after power up 100ms by different pull-up resistors of THERM and ALERT pin:

TEMPERATURE (°C)		THERM				
		2KΩ	7.5KΩ	10.5KΩ	14KΩ	18.7KΩ
ALERT#	2KΩ	77	87	97	107	117
	7.5KΩ	79	89	99	109	119
	10.5KΩ	81	91	101	111	121
	14KΩ	83	93	103	113	123
	18.7KΩ	85	95	105	115	125

### LID SENSOR



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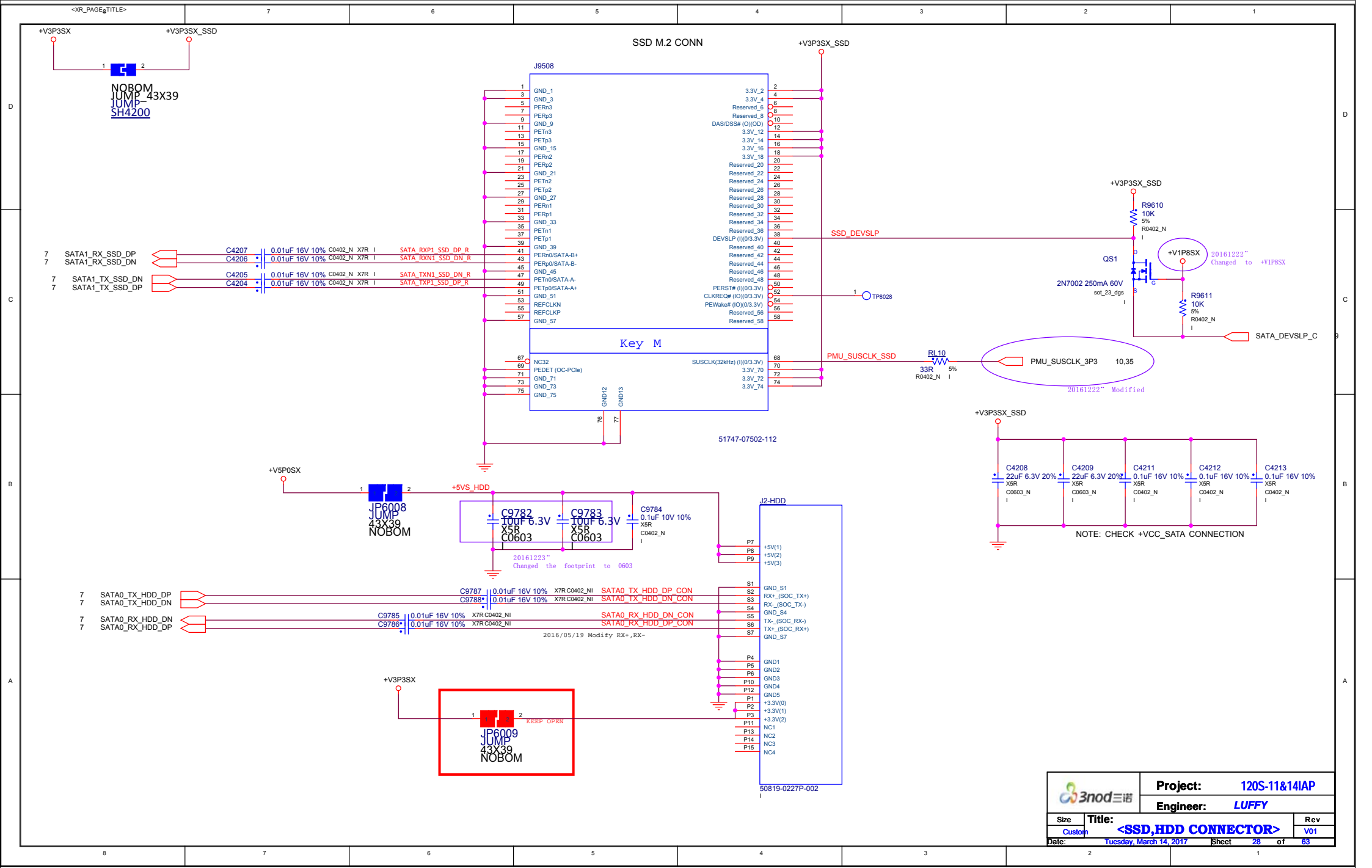
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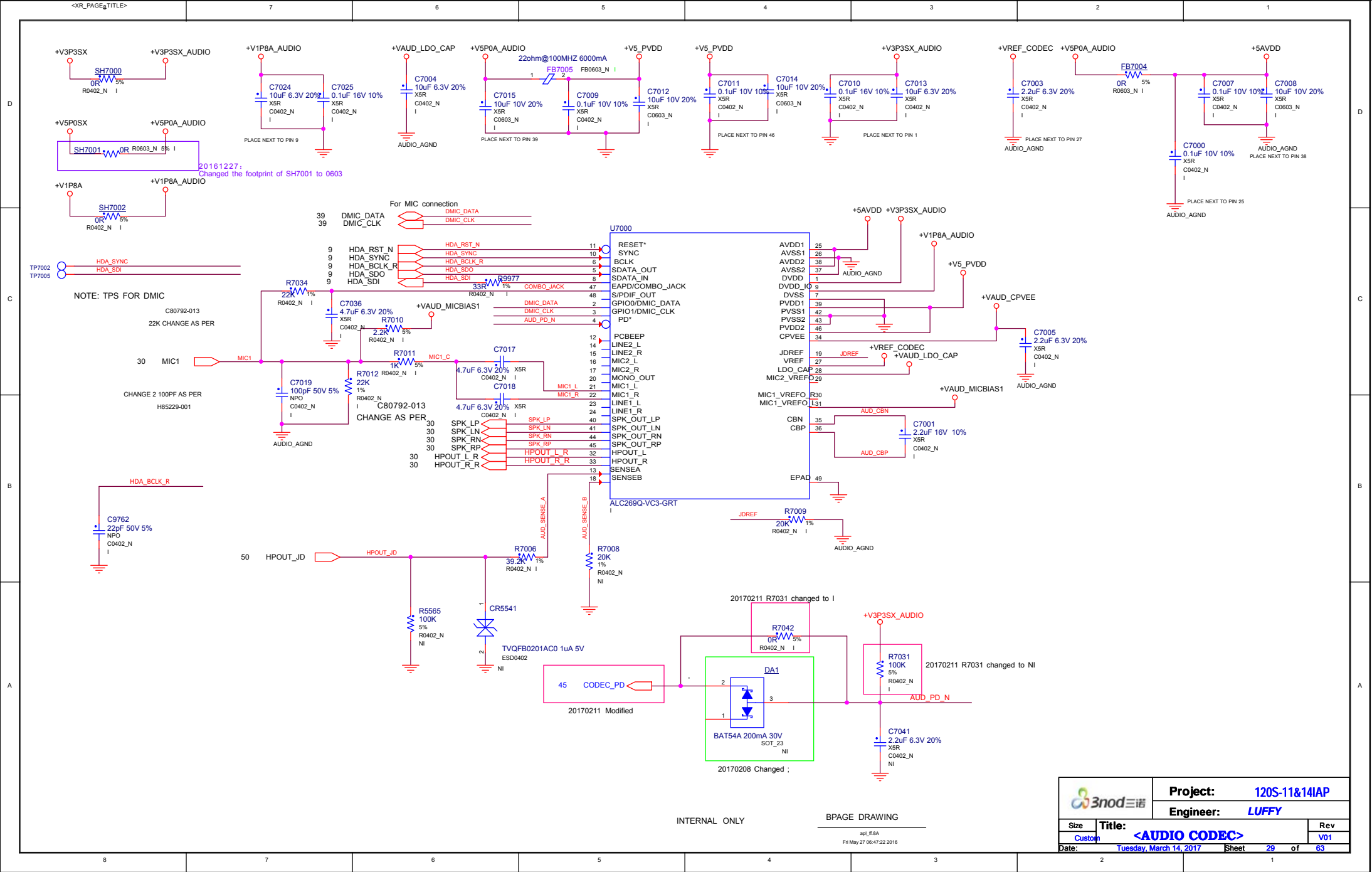
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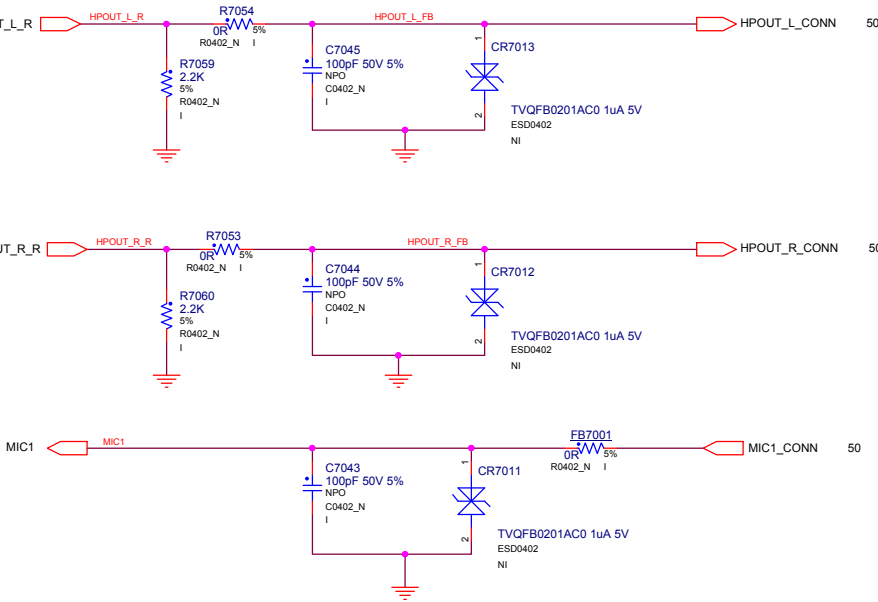
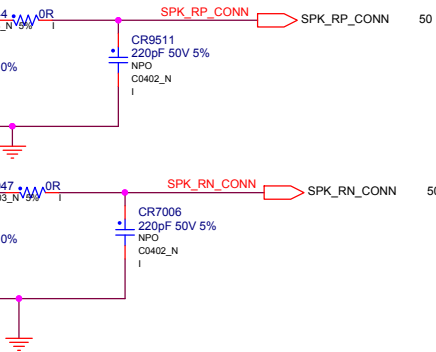
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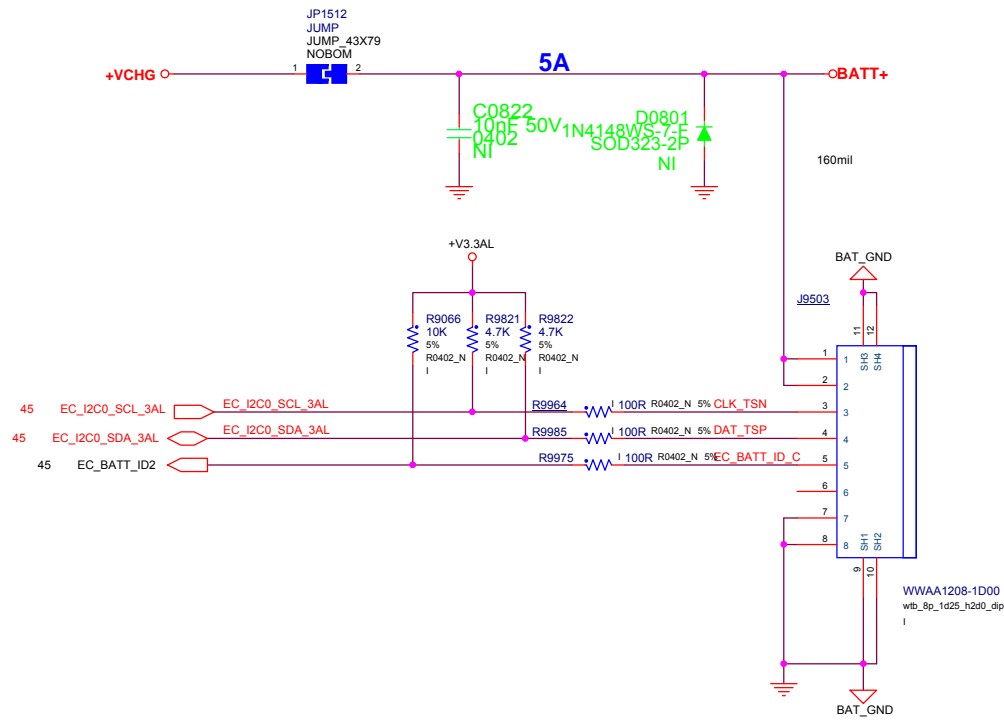


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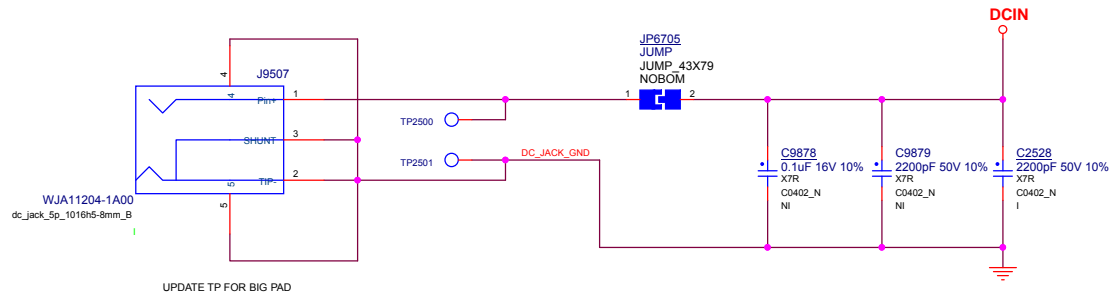
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20170205 Deleted reserved design for dummy battery


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B									B
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8	7	6	5	4	3	2	1		

INTERNAL ONLY

BPAGE DRAWING

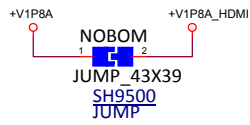
apl\_ft  
Fri May 27 06:47:24 2016

TYPE-C PD CONTROLLER

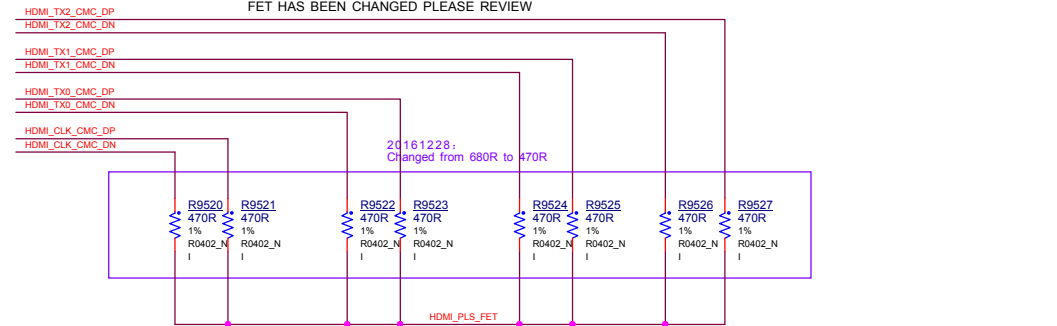
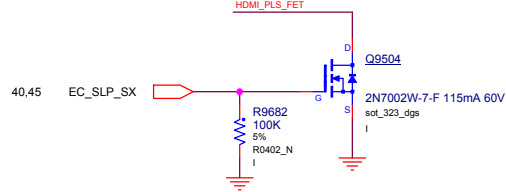
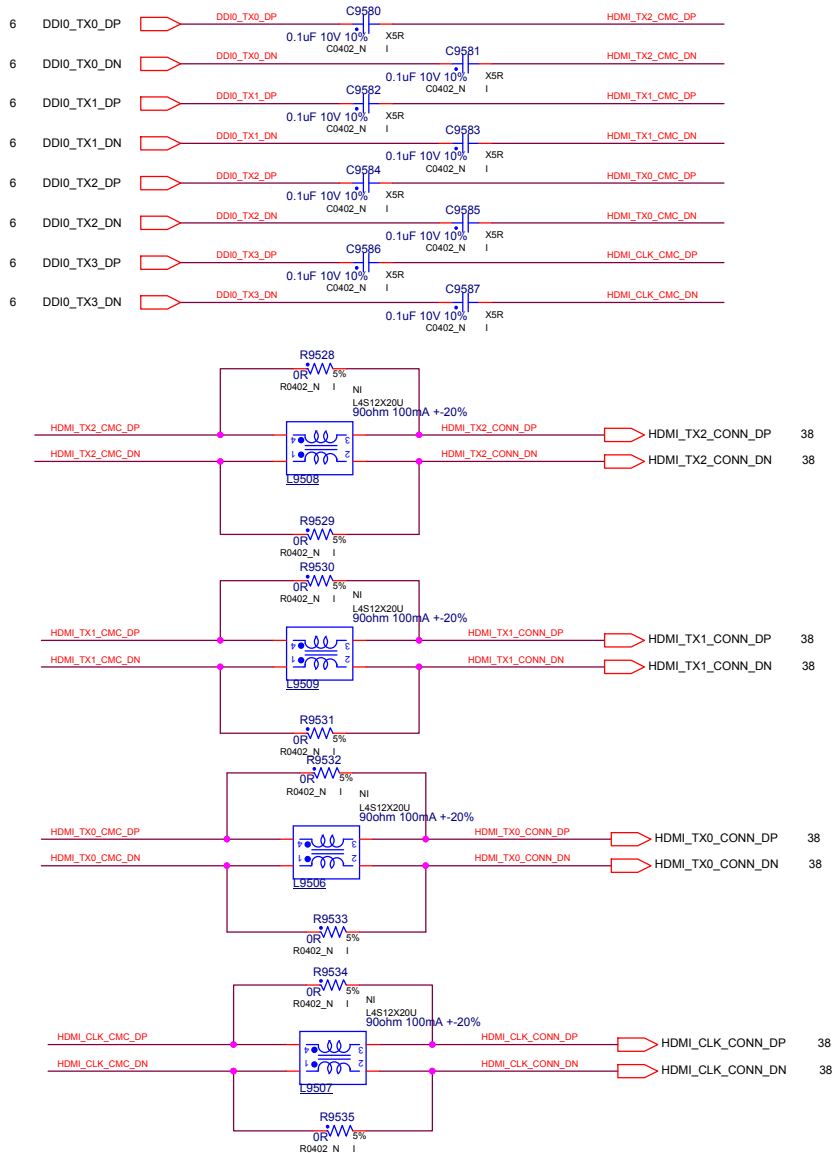
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		<b>Engineer:</b> LUFFY	
Size	<b>Title:</b> <NC>		Rev
Custom			V01
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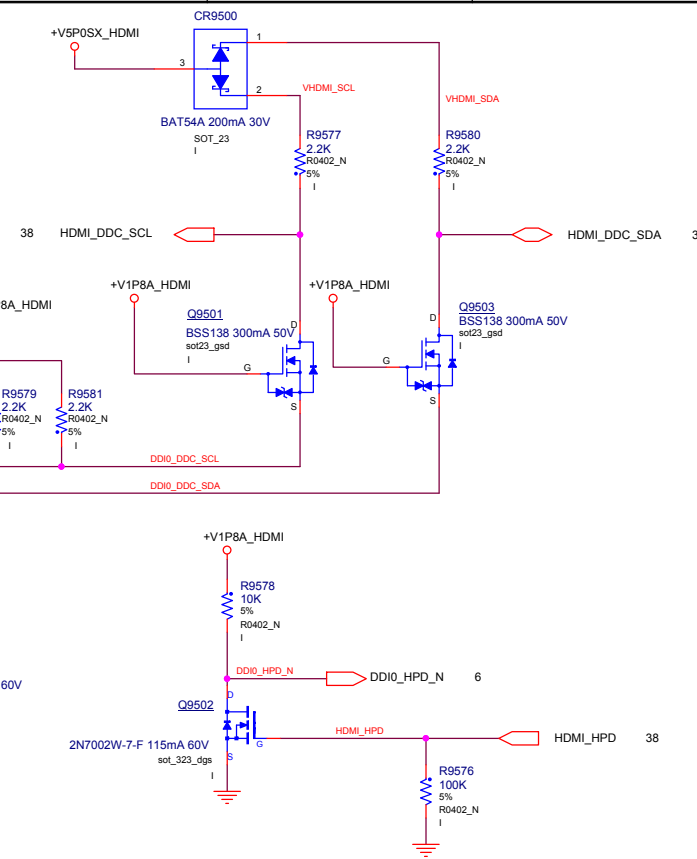


# HDMI LEVEL SHIFTER



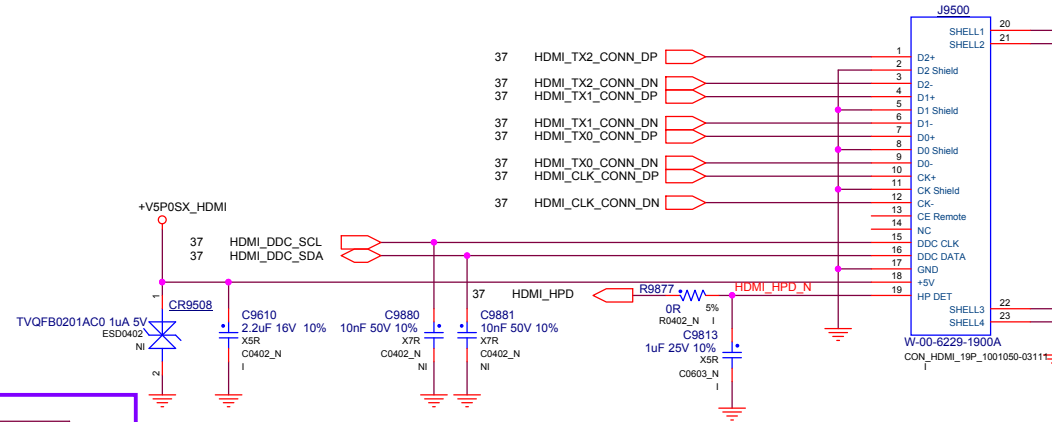
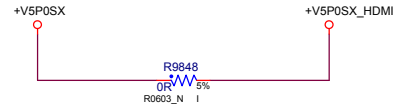
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sgl.83A  
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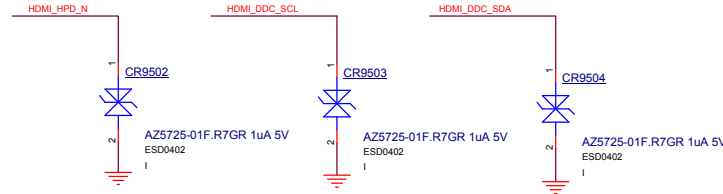
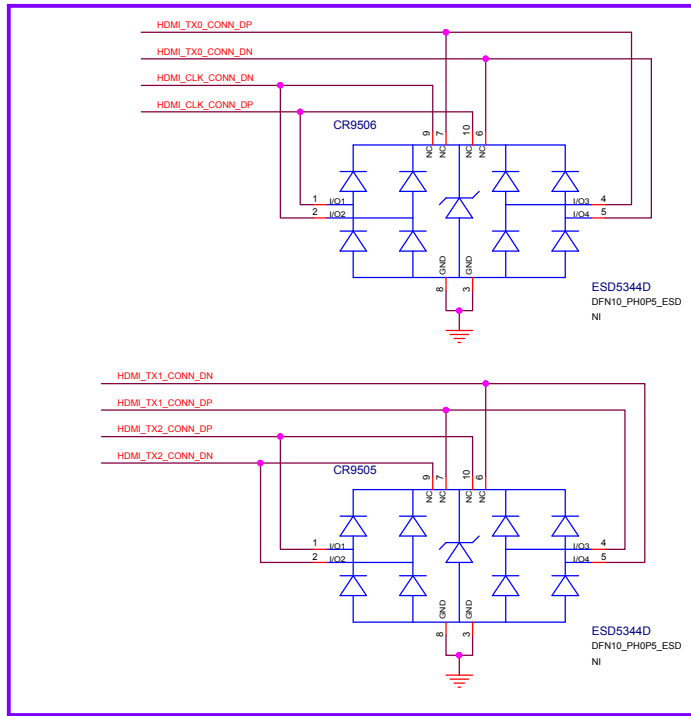


		Project: 120S-11&14IAP	
		Engineer: LUFFY	
Size	Title: <HDMI LEVEL SHIFTER>	Rev	V01
Customer			
Date: Tuesday, March 14, 2017	Sheet 37	of 63	

# HDMI CONNECTOR



20170314 CR9505/CR9506 changed to NI

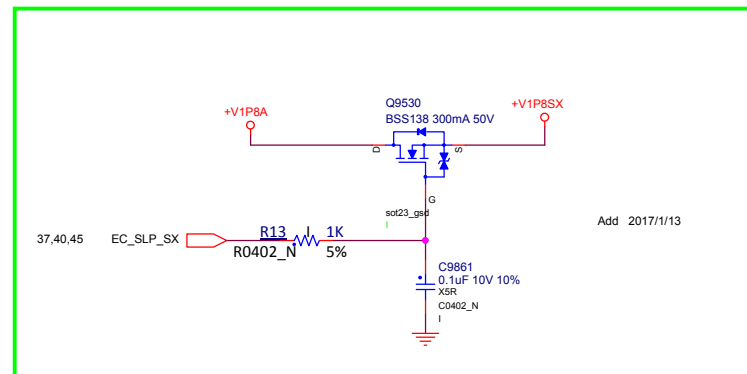
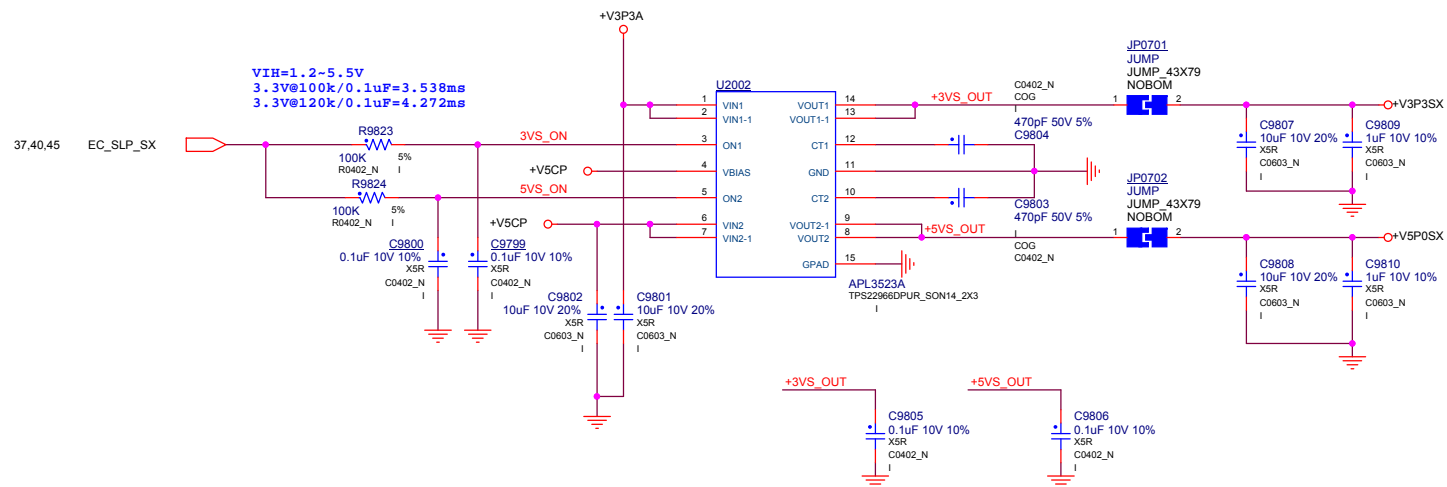


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991\_11\_1  
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		Project: 120S-11&14IAP	
		Engineer: LUFFY	
Size	Title: <HDMI CONN>	Rev	
Custom		V01	
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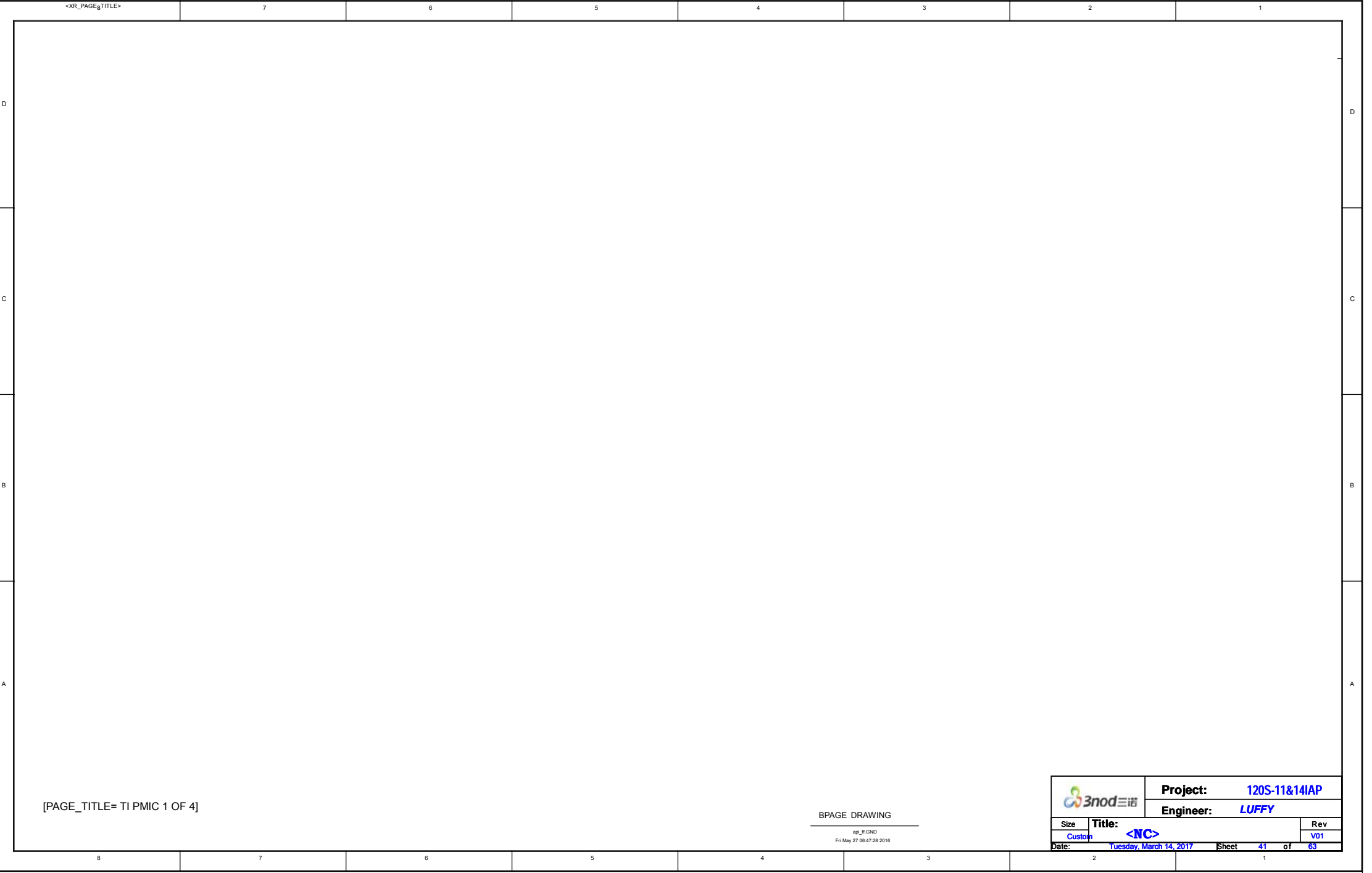


INTERNAL ONLY

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Size	Title:		
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[PAGE\_TITLE= TI PMIC 1 OF 4]

BPAGE DRAWING


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Fri May 27 06:47:26 2016

		Project: 120S-11&14IAP	
		Engineer: LUFFY	
Size	Title:	<NC>	Rev
Custom			V01
Date:	Tuesday, March 14, 2017	Sheet 41 of	63

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BPAGE DRAWING


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		<b>Engineer:</b> LUFFY	
Size	<b>Title:</b>		Rev
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<b>Date:</b> Tuesday, March 14, 2017		<b>Sheet</b> 42	<b>of</b> 63

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BPAGE DRAWING

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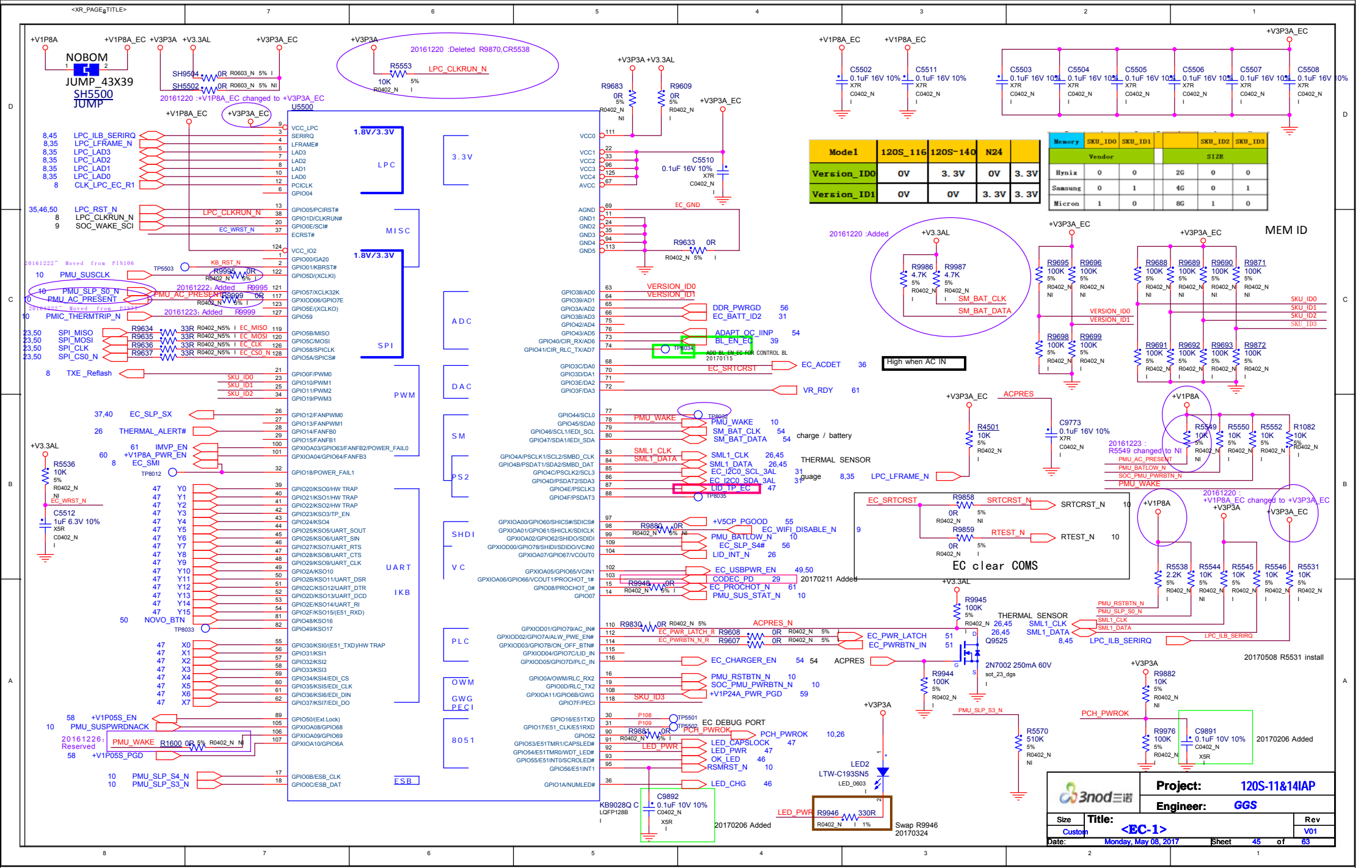


Project: 120S-11&14IAP

Engineer: LUFFY

Size	Title: <NC>	Rev
Custom		V01

Date: Tuesday, March 14, 2017 Sheet 44 of 63



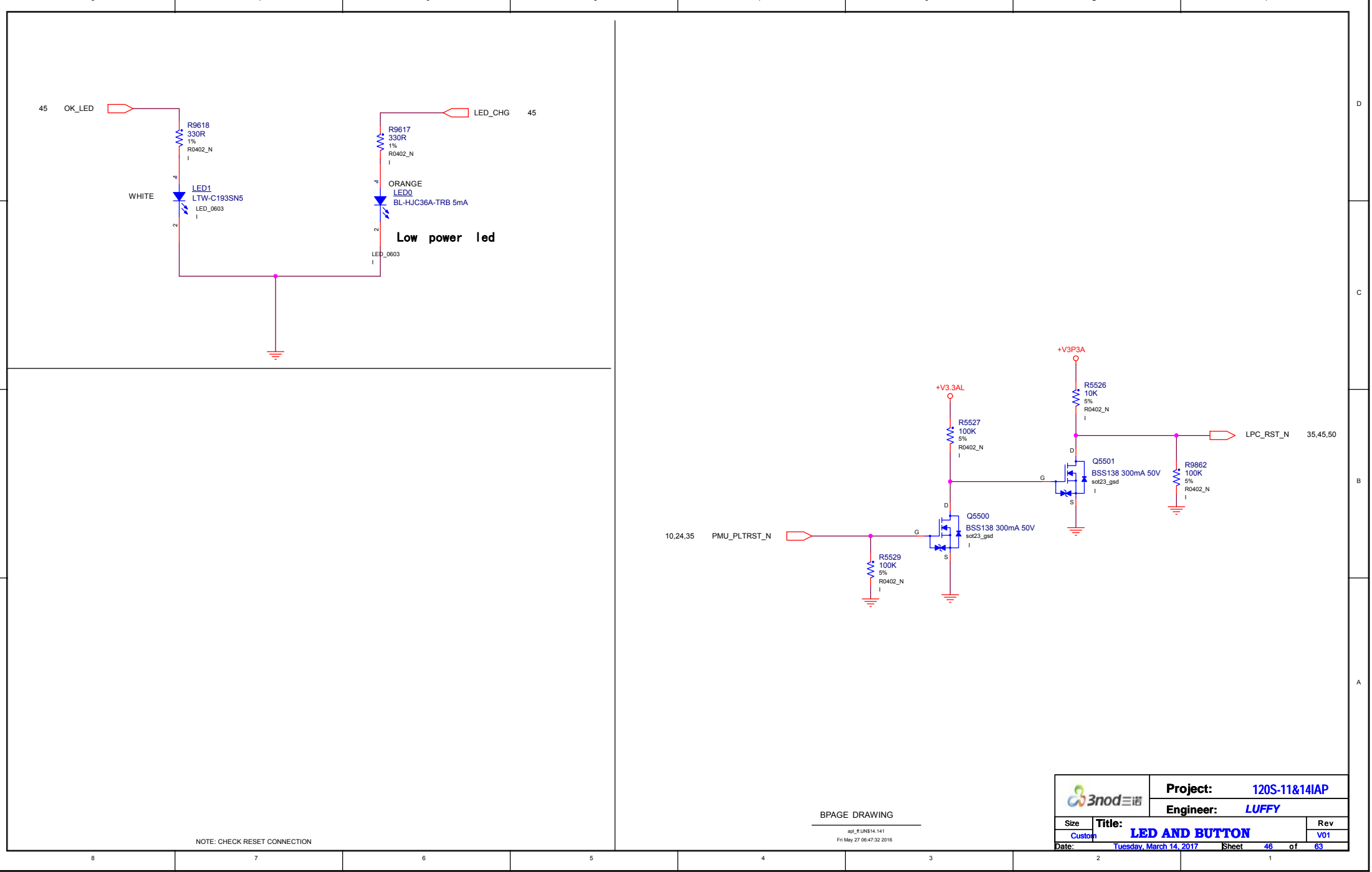
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Version_ID0	0V	3.3V	0V	3.3V
Version_ID1	0V	0V	3.3V	3.3V

Memory	SKU_ID0	SKU_ID1	SKU_ID2	SKU_ID3
Vendor	SIZE			
Hynix	0	0	2G	0
Samung	0	1	4G	0
Micron	1	0	8G	1

MEM ID

SKU_ID0	SKU_ID1	SKU_ID2	SKU_ID3
0	0	2G	0
0	1	4G	0
1	0	8G	1

Project: 120S-11&14IAP	
Engineer: GGS	
Size: Custom	Title: <EC-1>
Date: Monday, May 08, 2017	Rev: v01
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NOTE: CHECK RESET CONNECTION

BPAGE DRAWING

apl\_8.LIN\$14.141  
Fri May 27 06:47:32 2016



Project: 120S-11&14IAP

Engineer: LUFFY

Size	Title: LED AND BUTTON	Rev
Custom		V01

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D

D

C

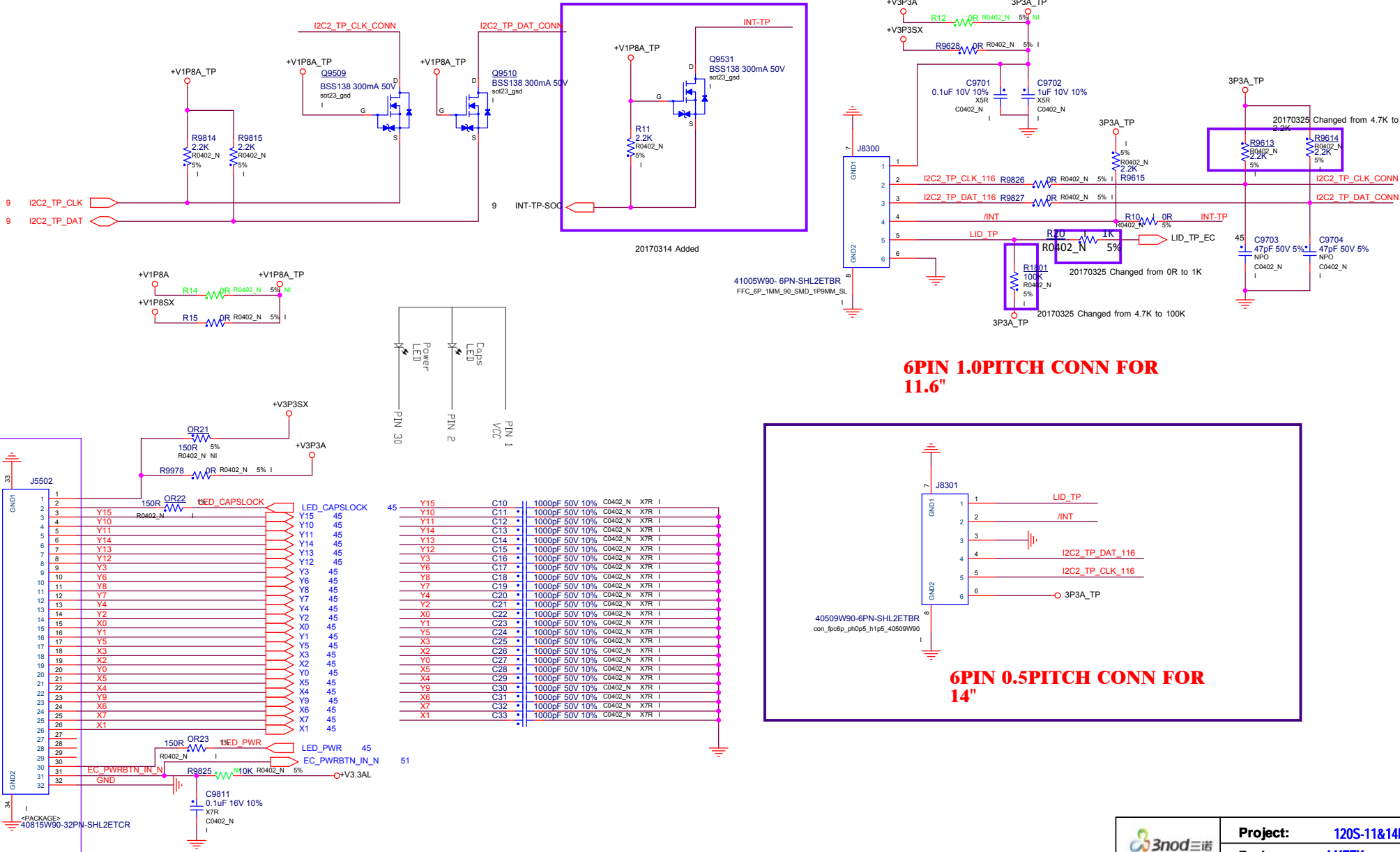
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INTERNAL ONLY

BPAGE DRAWING


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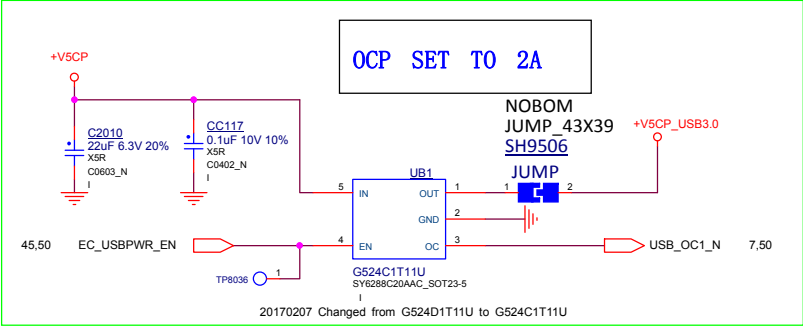
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		Engineer:	LUFFY
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Date:	Monday, May 08, 2017	Sheet	47 of 63

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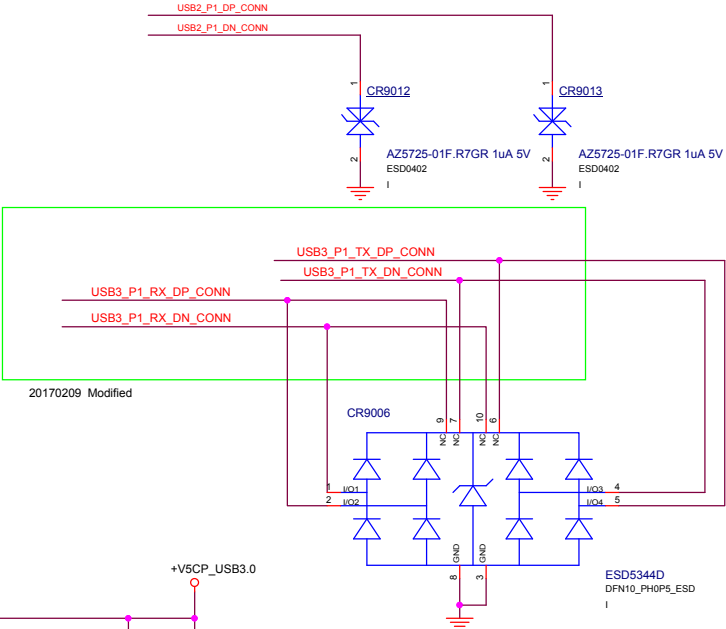
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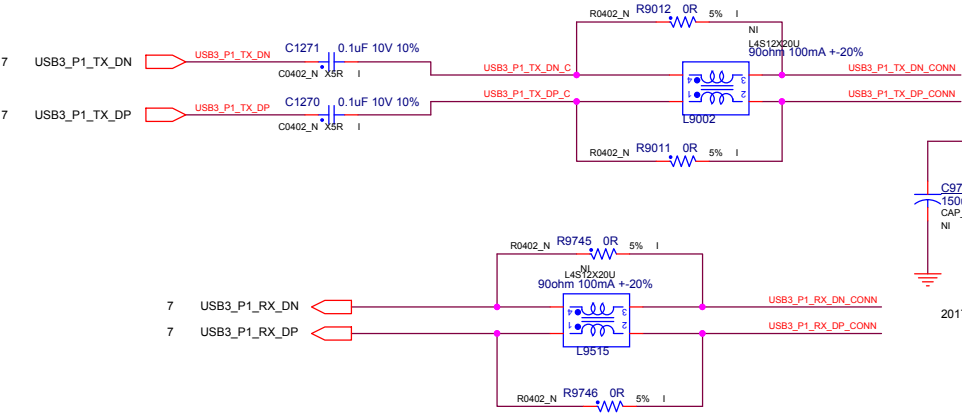
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Size	<b>Title:</b> <NC>		Rev
Custom			V01
<b>Date:</b> Tuesday, March 14, 2017		<b>Sheet</b> 48	<b>of</b> 63



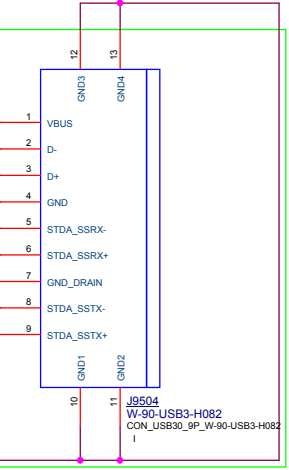
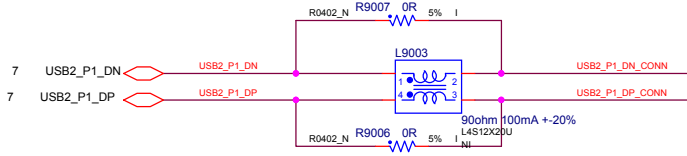
20170206 Modified



20170209 Modified



20170314 Added C9900/C9902; C9791 changed to NI; C9007 changed to I



20170206 changed

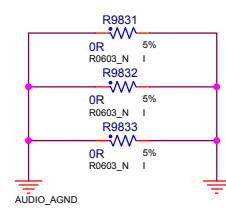
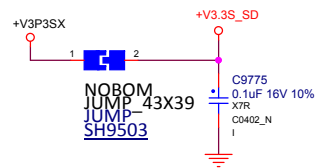
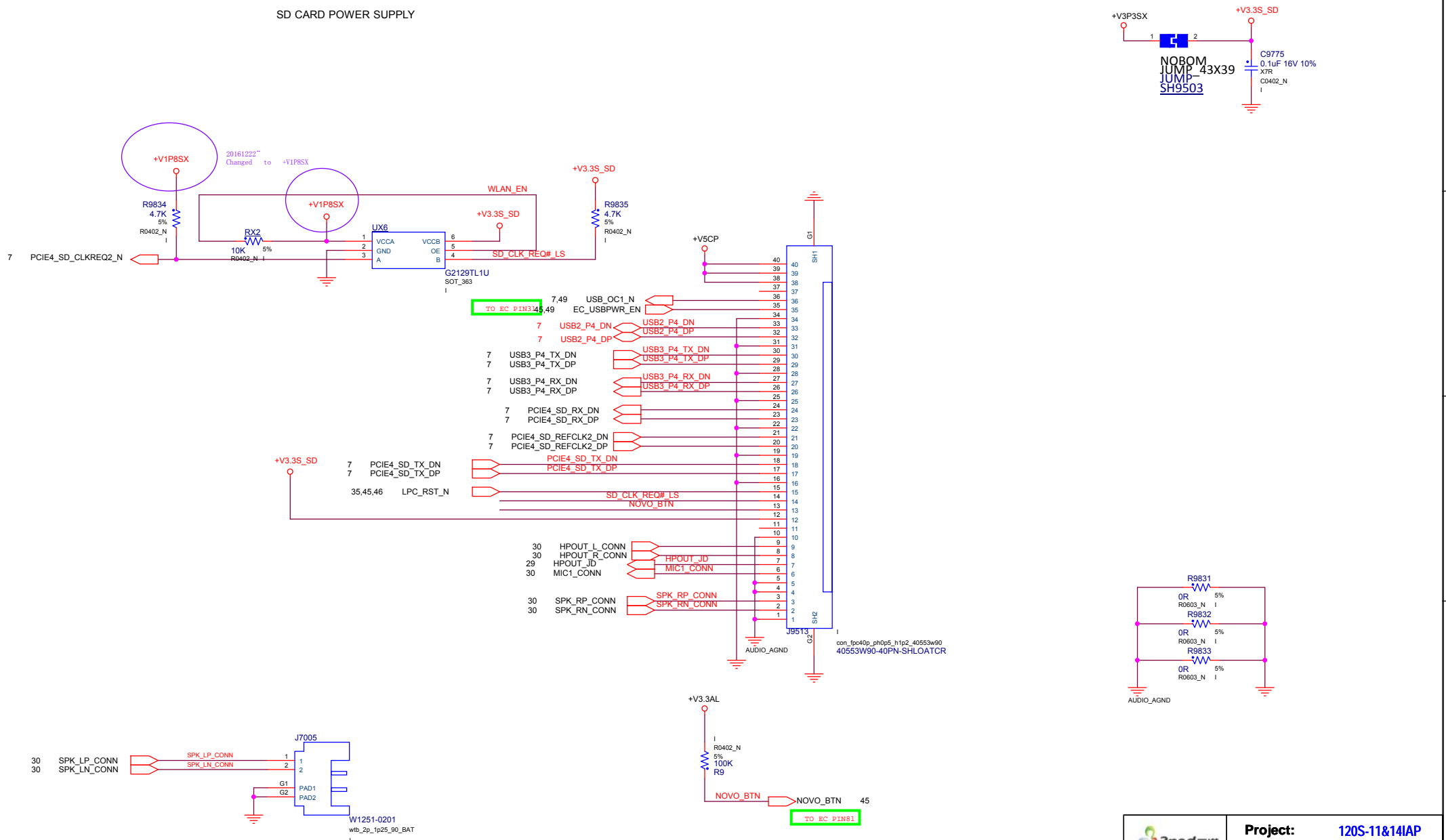
INTERNAL ONLY

BPAGE DRAWING

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Size	Title:	Rev	
Custom	USB CHANGER,USB3.0 CONN		01
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# SD CARD POWER SUPPLY



BPAGE DRAWING

apl\_If.s  
Fri May 27 06:47:32 2016

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		Engineer:	LUFFY
Size	Title:	Rev	
Custom	<IO&DEBUG CONN>	V01	
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INTERNAL ONLY

BPAGE DRAWING


apf\_8 UN\$20.205  
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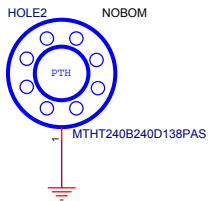
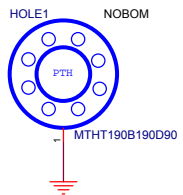
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Size	<b>Title:</b> <NC>		Rev
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Date:	Tuesday, March 14, 2017		Sheet 52 of 63

INTERNAL ONLY

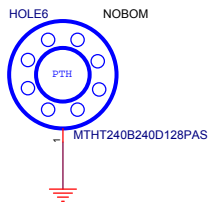
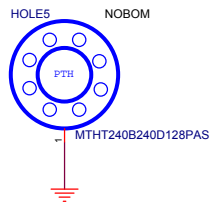
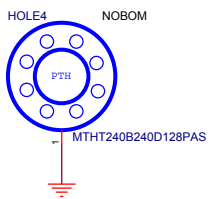
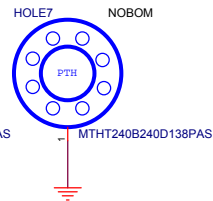
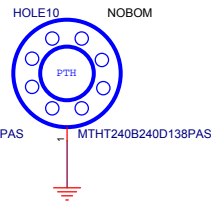
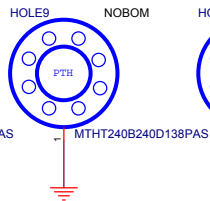
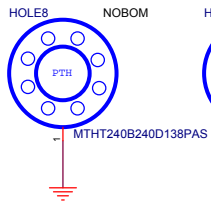
BPAGE DRAWING

apl\_E UN\$20.205  
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		Project: 120S-11&14IAP	
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Size	Title:	Rev	
Custom	<NC>	V01	
Date:	Tuesday, March 14, 2017	Sheet	52 of 63




20170323 Del HOLE 3



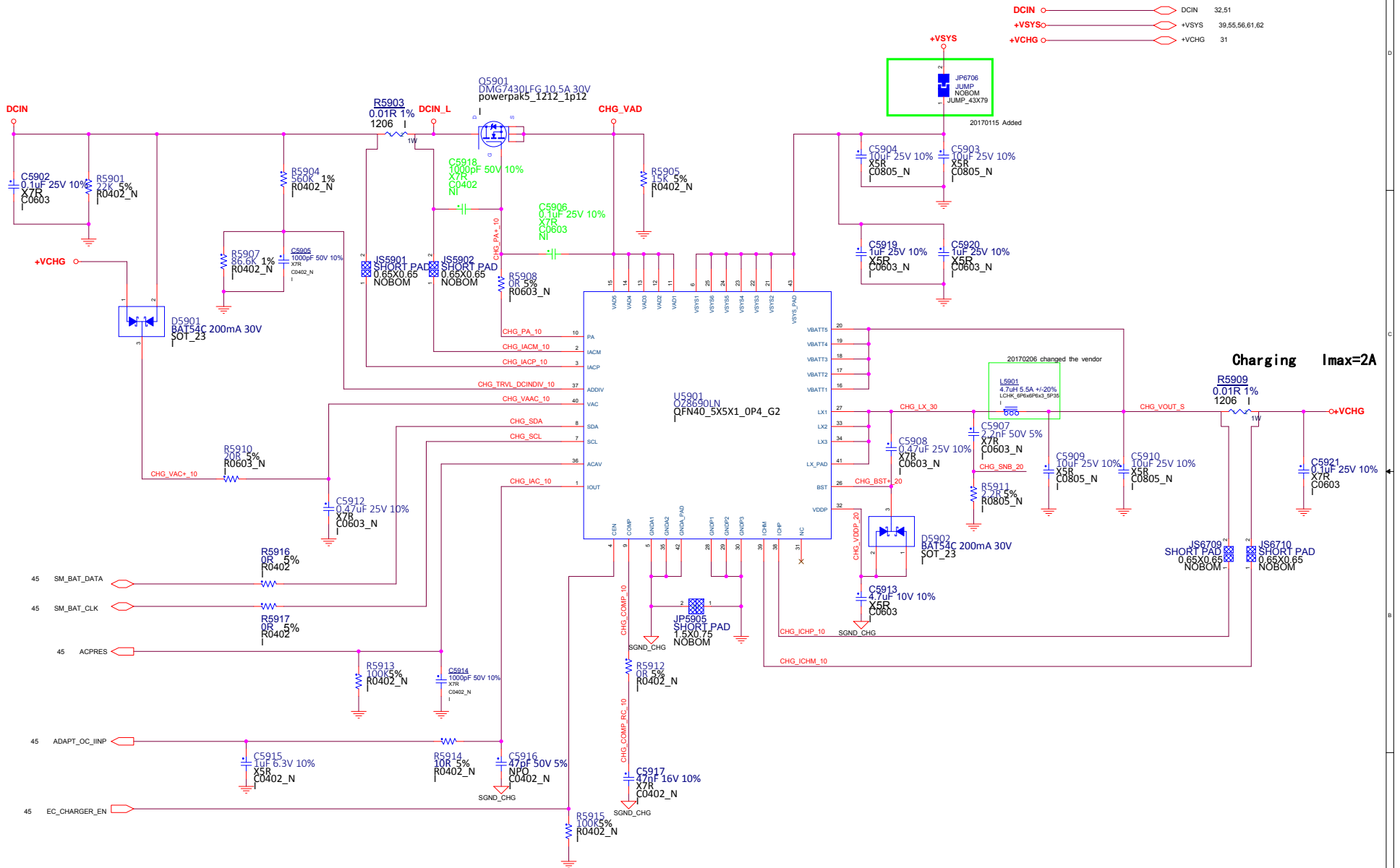
INTERNAL ONLY

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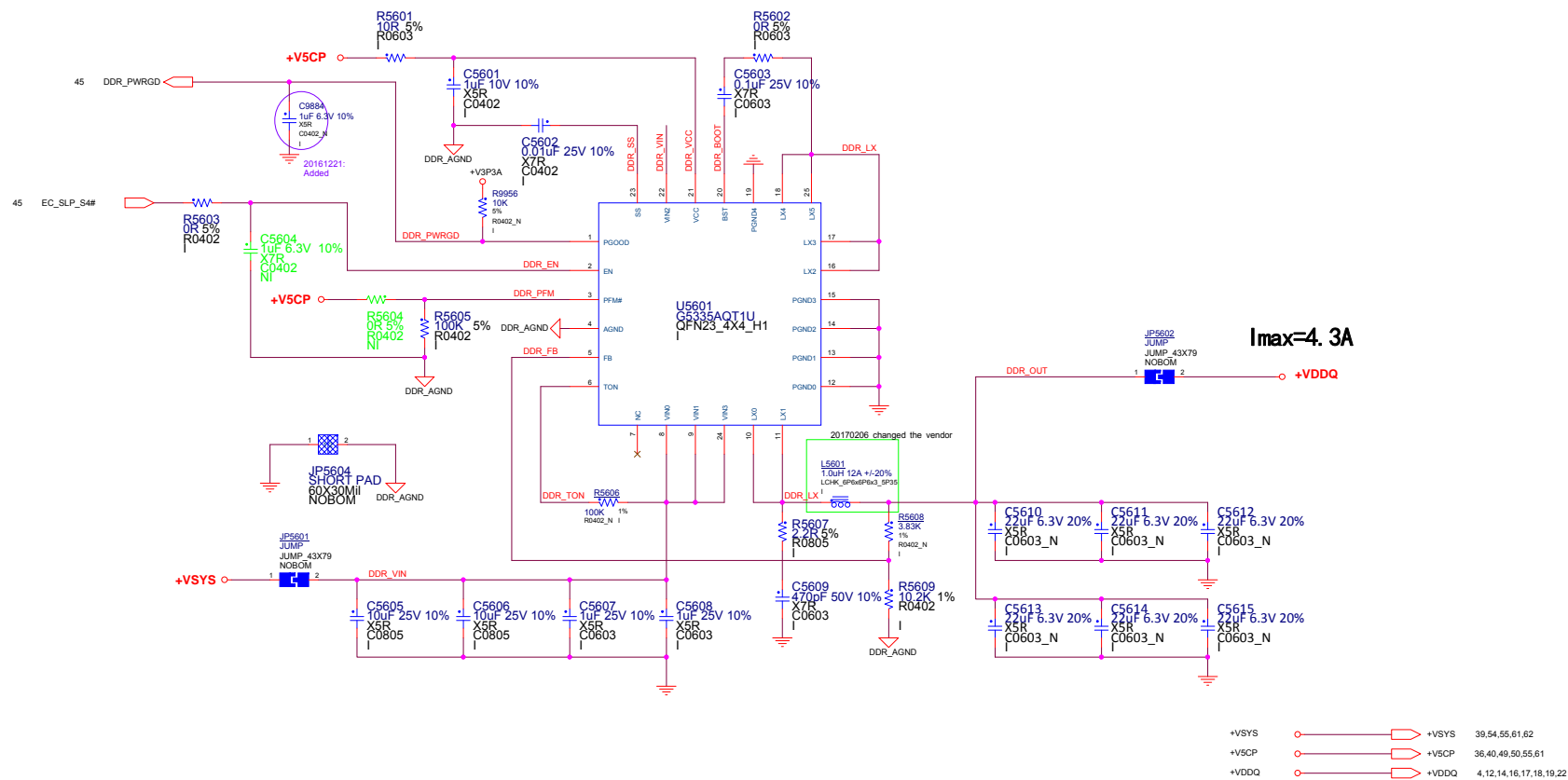
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Size	Title: <SCREW>	Rev	
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Date: Friday, March 24, 2017	Sheet 53 of 63		V01

## 59: BATTERY CHARGER






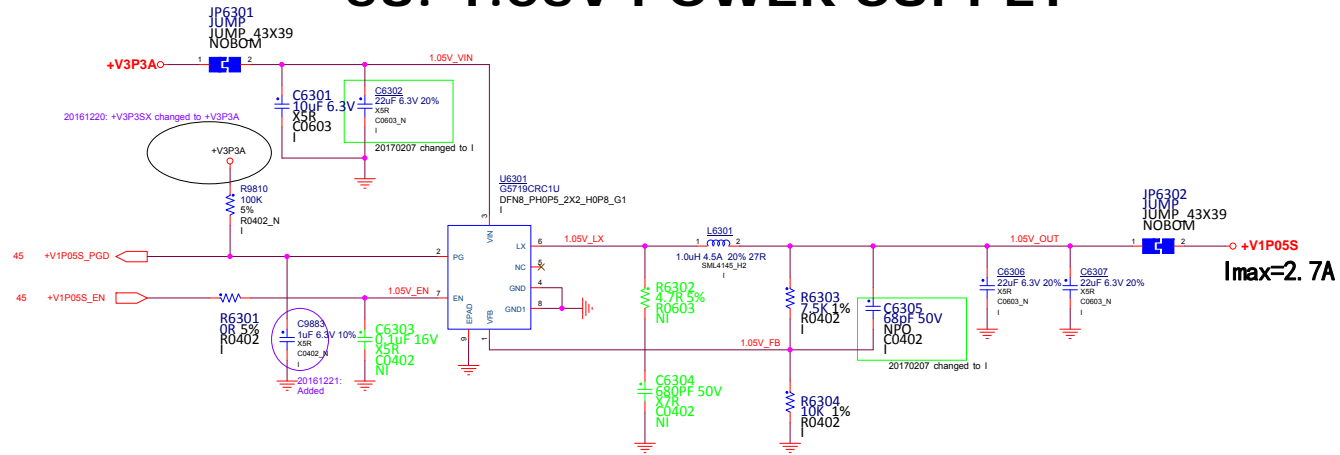
# 56: DDR POWER SUPPLY



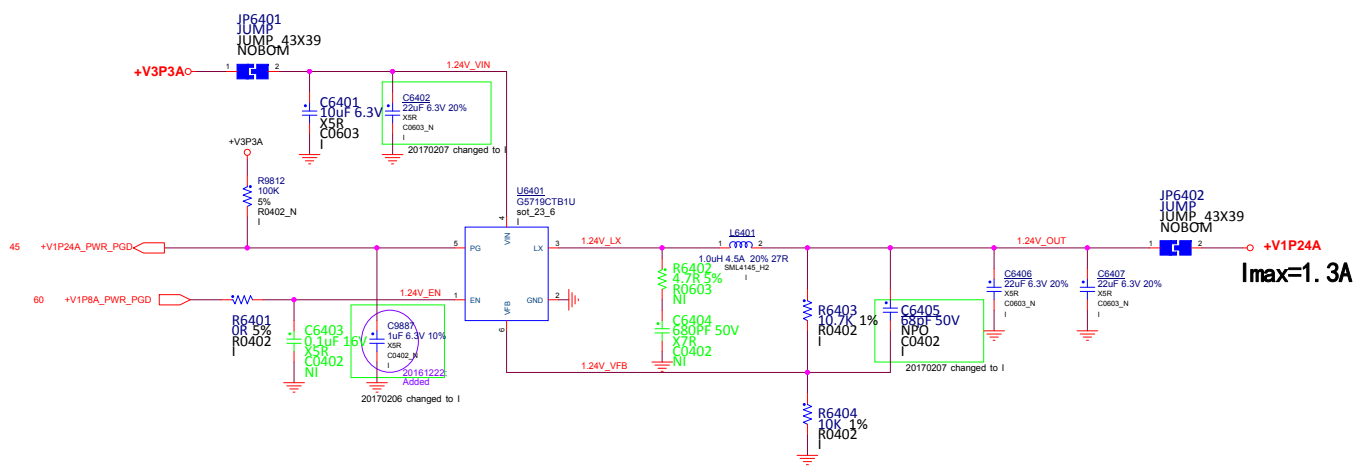
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		Project: 120S-11&14IAP	
		Engineer: Frank	
Size	Title:		Rev
C	<NC>		V01
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# 58: 1.05V POWER SUPPLY

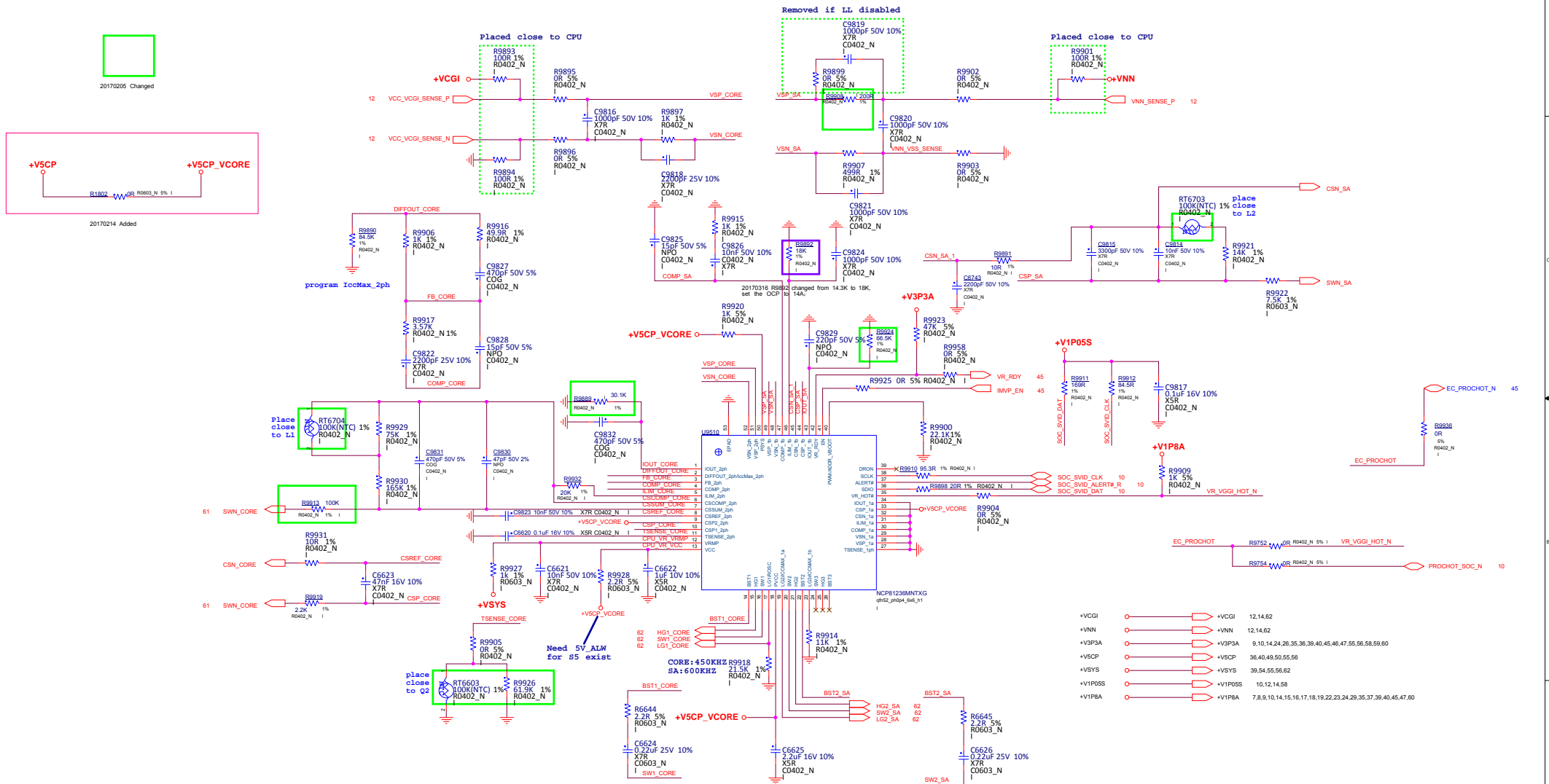


# 59: 1.24V POWER SUPPLY

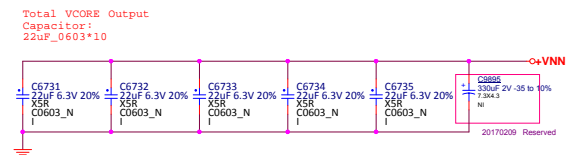
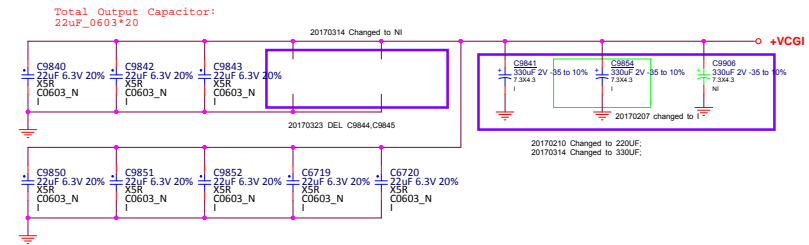
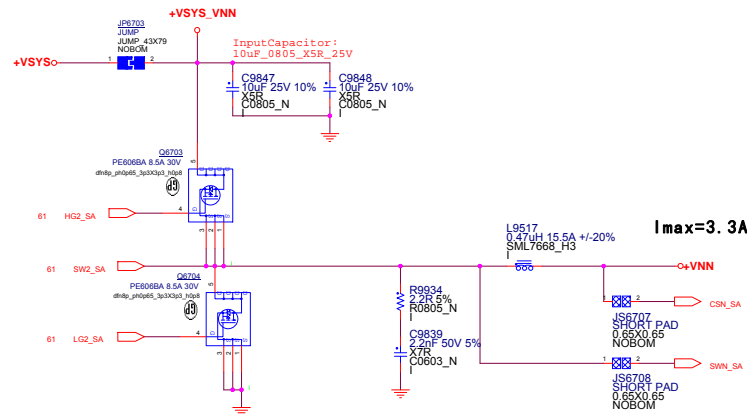
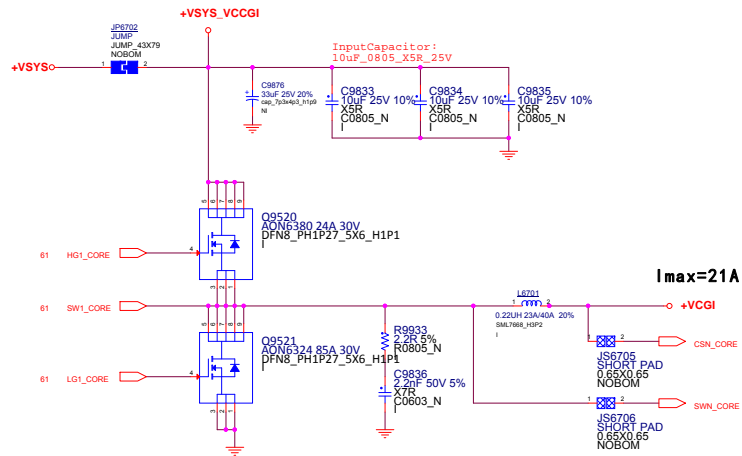




# CPU POWER SUPPLY



# VCGI /VNN POWER SUPPLY



+VCGI	○	○	+VCGI	12,14,61
+VNN	○	○	+VNN	12,14,61
+VSYS	○	○	+VSYS	39,54,55,56,61

		<b>Project:</b> 120S-11&14IAP	
		<b>Engineer:</b> Frank	
<b>Size</b>	<b>Title:</b> <PWR BLOCK DIAGRAM>	<b>Rev</b>	
C		V01	
<b>Date:</b>	Tuesday, March 14, 2017	<b>Sheet</b>	63 of 63